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HSF Property:ROHS or Halogen-Free

COMET DIS

SI1 BUILD

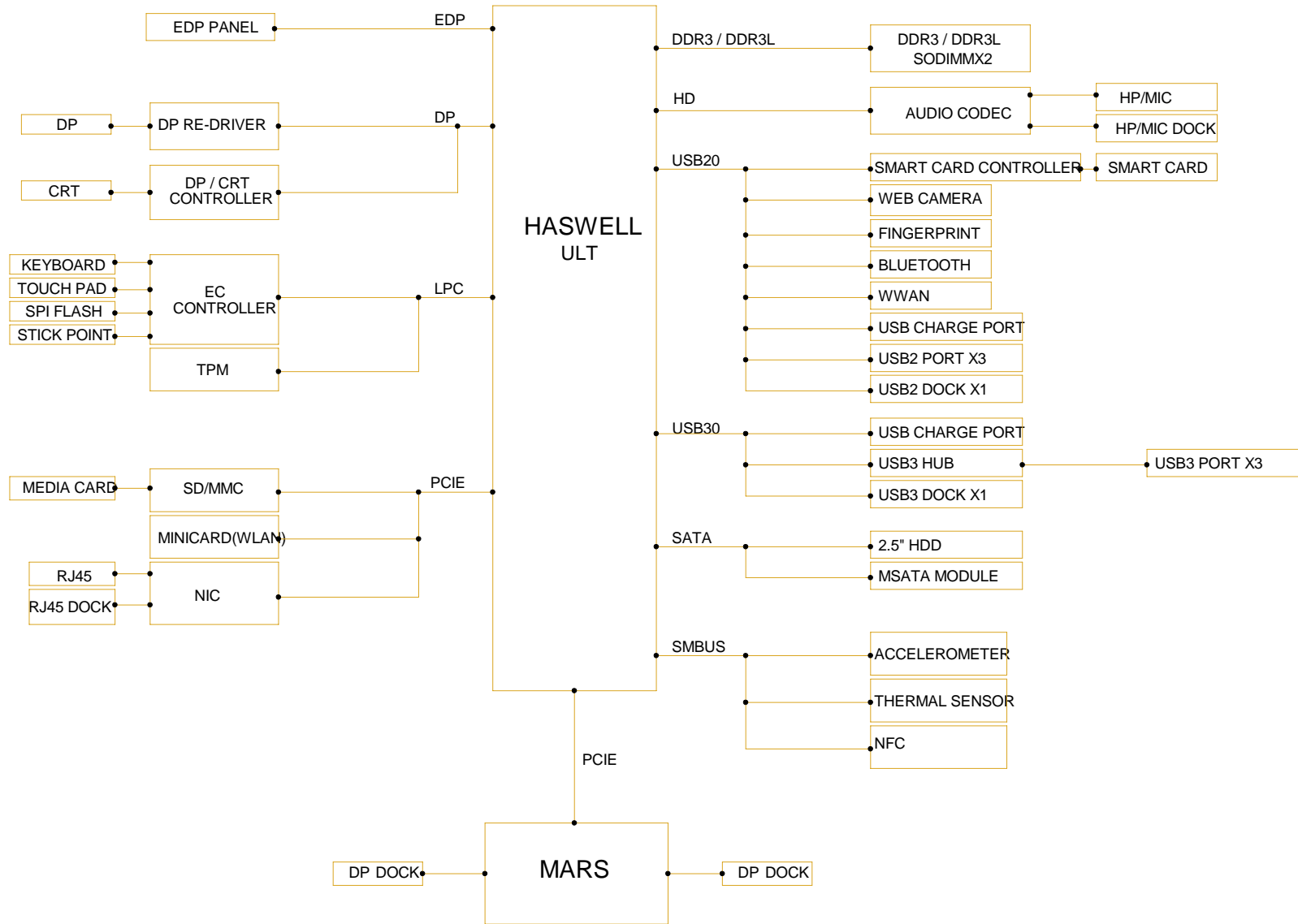
2012.11.30

21-OCT-2002		
DATE	CHANGE NO.	REV

INVENTEC					
DRAWER	EE	DATE	POWER	DATE	
DESIGN	isa chen	2012/10/24	isa chen	2012/10/24	
CHECK	isa chen	2012/10/24	isa chen	2012/10/24	
RESPONSIBLE	isa chen	2012/10/24	isa chen	2012/10/24	
SIZE: A4					VER: x01
FILE NAME: COMET DIS					SIZE: 5
PIN: xxxxxxxxxxxx					CODE: CS
					DOC NUMBER: 6310xxxx-0-0
					REV: x01
					SHEET: 1 of 17

PRIMARY LI-LON BATTERY
SECOND LI-LON BATTERY

SIDE DOCK CONNECTOR

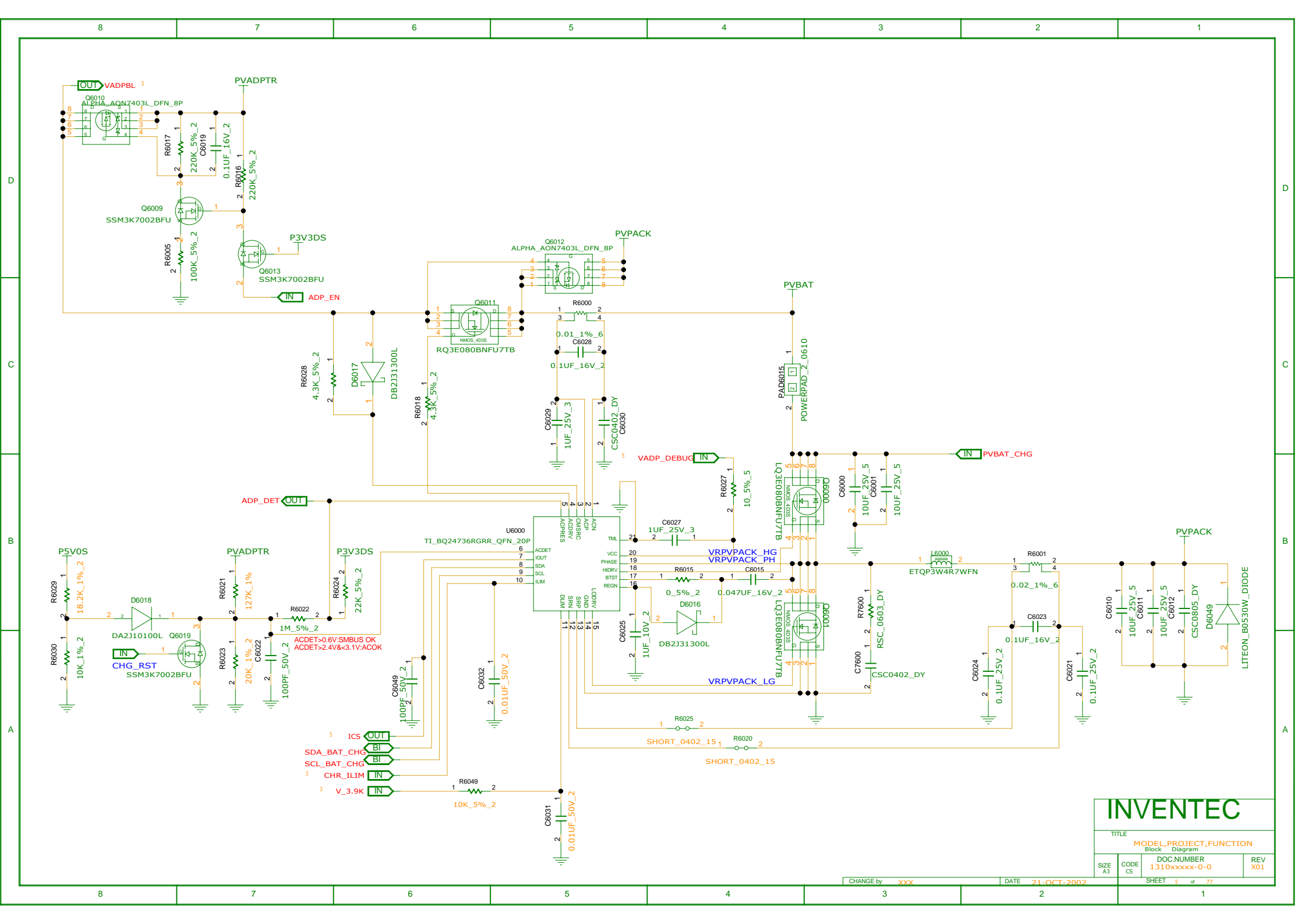


INVENTEC				
TITLE				
MODEL, PROJECT, FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
C	CS	131000000-0-0	201	
CHANGE BY		DATE	SHEET	
XXX		21-OCT-2002	1 of 07	

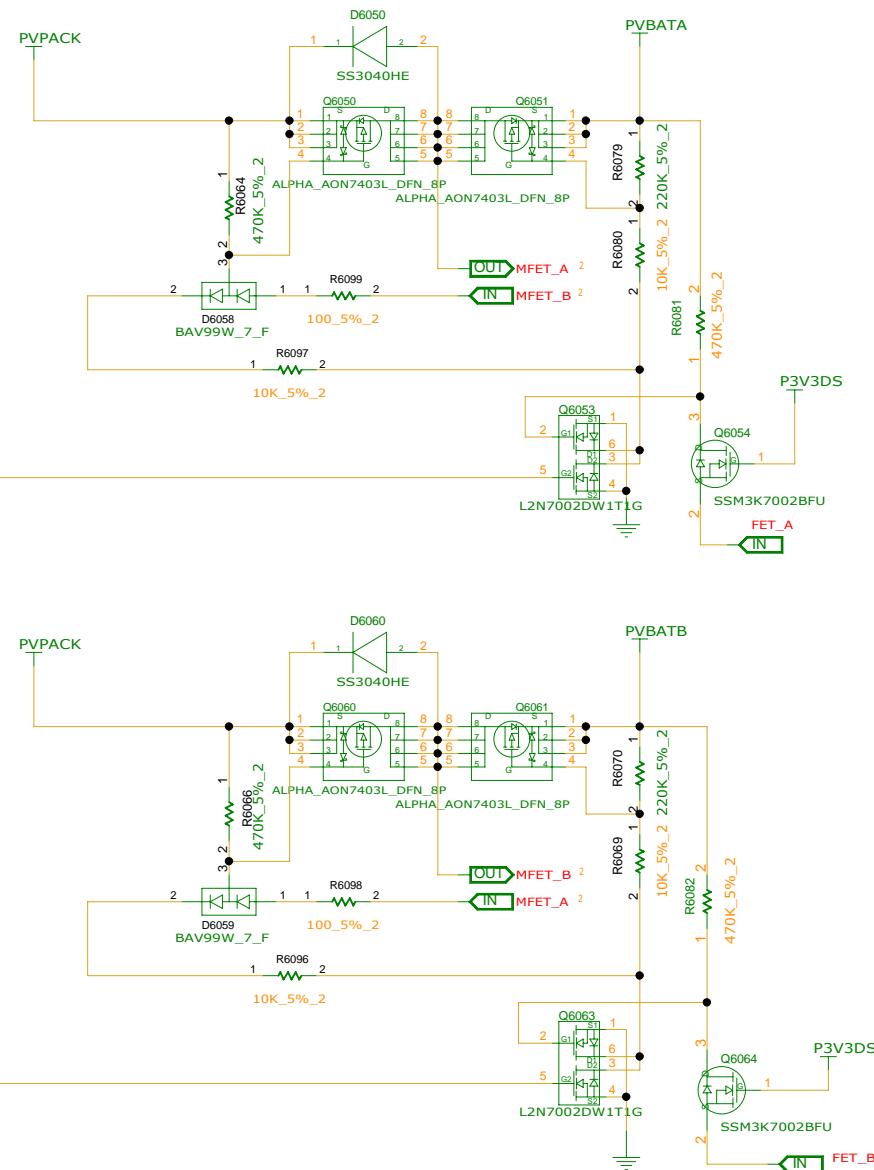
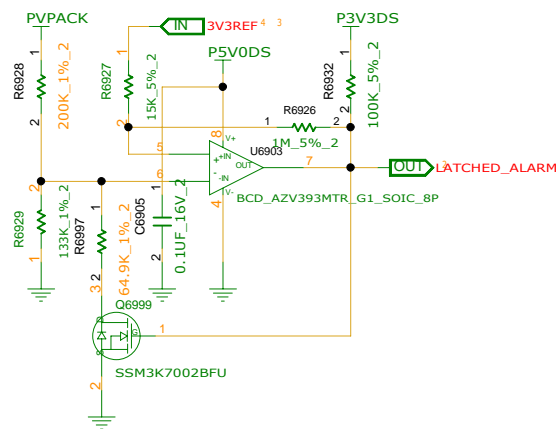
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02.BLOCK DIAGRAM	27.HASWELL_1 (MISC,JTAG)	52.KEYBOARD
03.TABLE OF CONTENTS	28.HASWELL_2 (LPC,SPI,SMBUS,CLINK,PM)	53.TPM
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05.SYSTEM POWER(CHARGER)	30.HASWELL_4 (DP,EDP)	55.WLAN/BT SLOT
06.SYSTEM POWER(BATT SELECTOR)	31.HASWELL_5 (DDR)	56.WWAN SLOT, SIM SLOT
07.SYSTEM POWER(OCF)	32.HASWELL_6 (PCIE,USB)	57.DOCKING
08.SYSTEM POWER(P3V3A&P5V0A)	33.HASWELL_7 (RTC,AUDIO,SATA,JTAG)	58.B TO B CONN, POINT STICK CONN
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10.SYSTEM POWER(P1V5)	35.HASWELL_9 (POWER)	60.AUDIO JACK, MIC AMP.
11.SYSTEM POWER(P1V05_M)	36.HASWELL_10 (POWER)	61.CARD READER
12.SYSTEM POWER(P1V05S)	37.HASWELL_11 (GND)	62.BUTTON, LED
13.USB HUB POWER (P1V2A)	38.SYSTEM MEMORY (DIMM0)	63.SMART CARD DAUGHTER BOARD
14.SYSTEM POWER(PVCORE&PVAXG-1)	39.SYSTEM MEMORY (DIMM1)	64.CRT DB WTB CONN
15.SYSTEM POWER(PVCORE&PVAXG-2)	40.EMPTY	65.MIC DB
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17.DC JACK & BATTERT CONN.	42.DP TO VGA CONVERTER	67.EMPTY
18.HP_OCP	43.DISPLAY PORT	68.MARS-1
19.PVCORE_DGPU	44.LCM & WEBCAM CONN	69.MARS-2
20.PVDDCI	45.SATA HDD, MSATA	70.MARS-3
21.P1V35S_DGPU	46.USB HUB	71.MARS-4
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TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

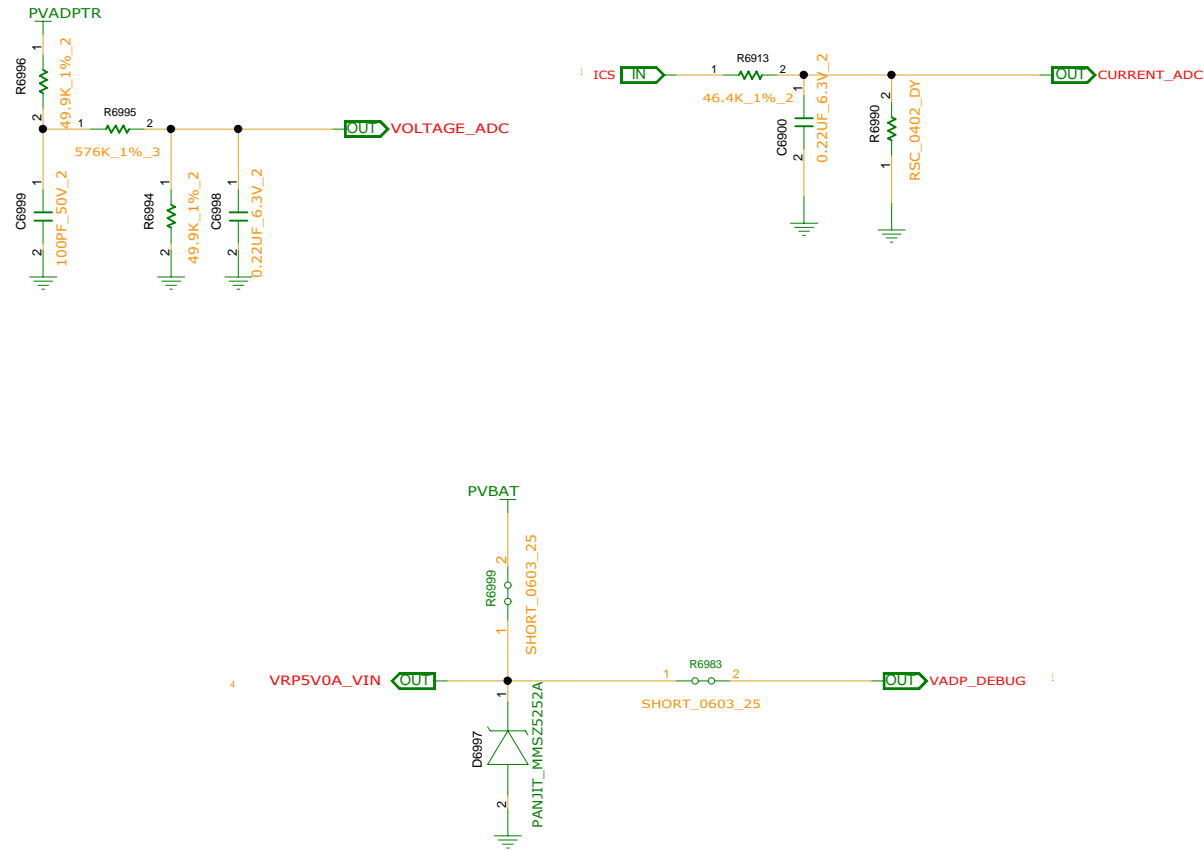


INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
	Block Diagram

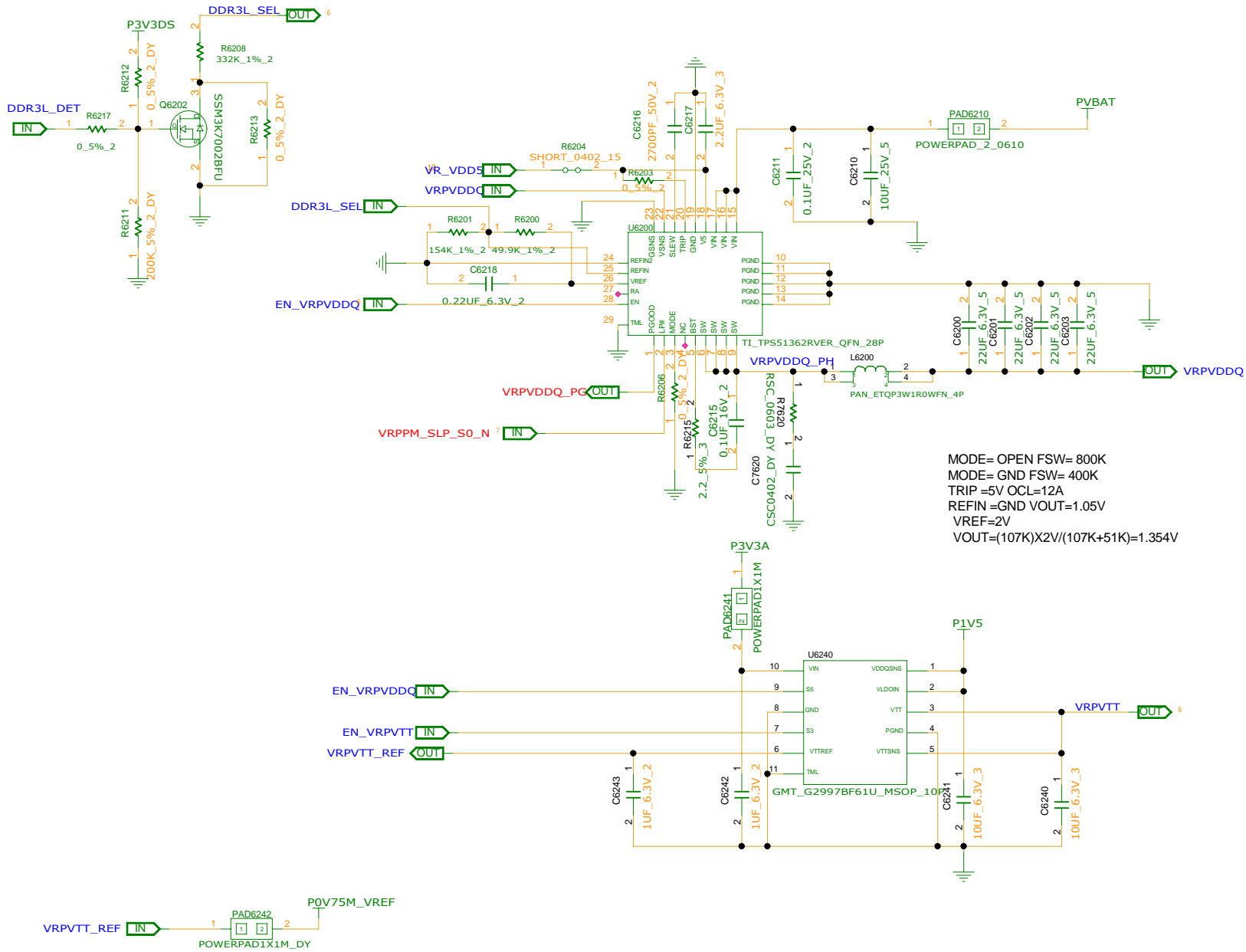
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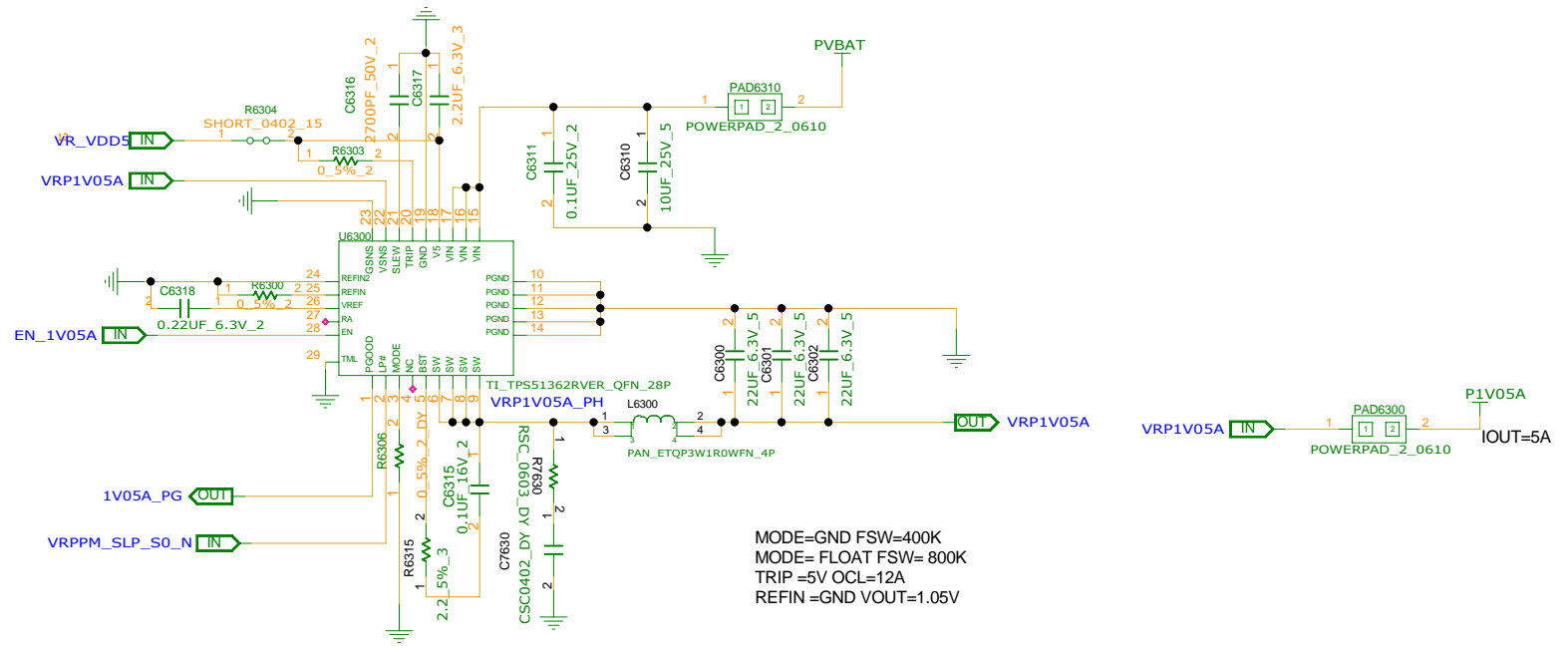
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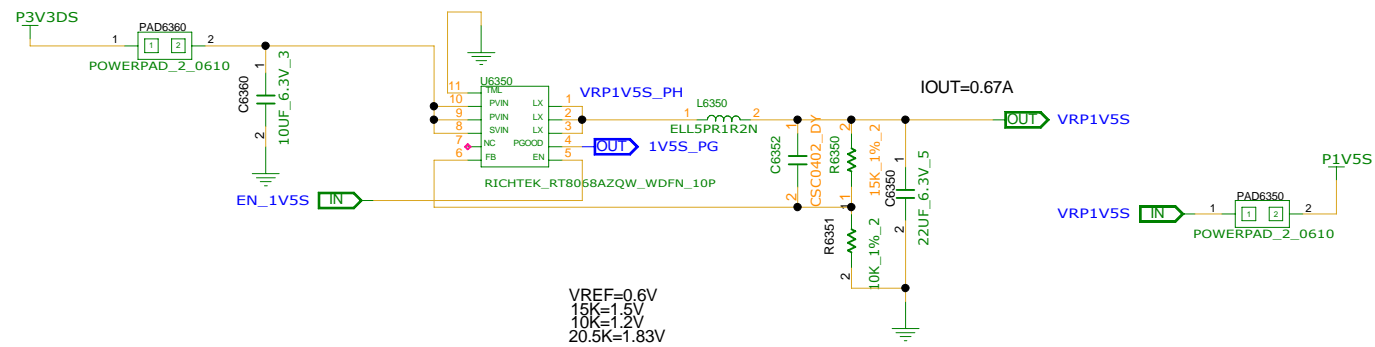
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01



MODE= OPEN FSW= 800K
 MODE= GND FSW= 400K
 TRIP =5V OCL=12A
 REFIN =GND VOUT=1.05V
 VREF=2V
 $VOUT=(107K) \times 2V / ((107K+51K)=1.354V$

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
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A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	SHEET
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INVENTEC

TITLE
MODEL,PROJECT,FUNCTION

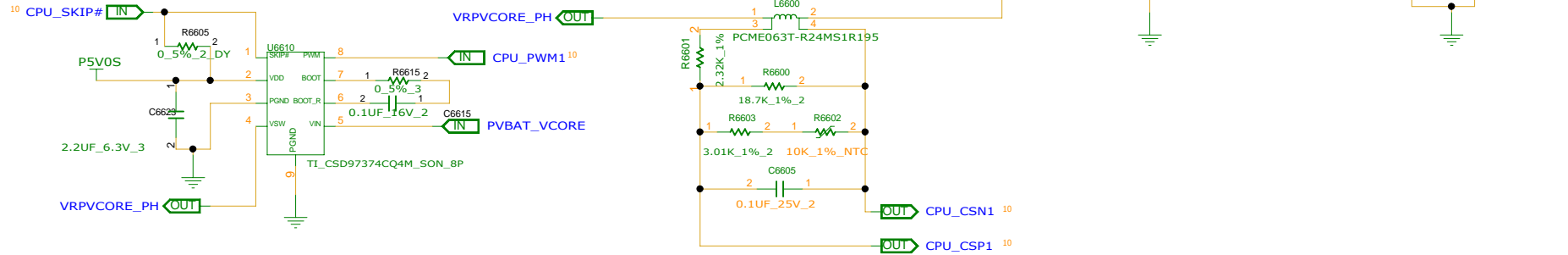
Block Diagram

DOC NUMBER
1310xxxxx-0-0

REV
X01

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CHANGE by XXX DATE 21-OCT-2002



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

[illegible]

TITLE			
MODEL,PROJECT,FUNCTION			
Block		Diagram	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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D

D

C

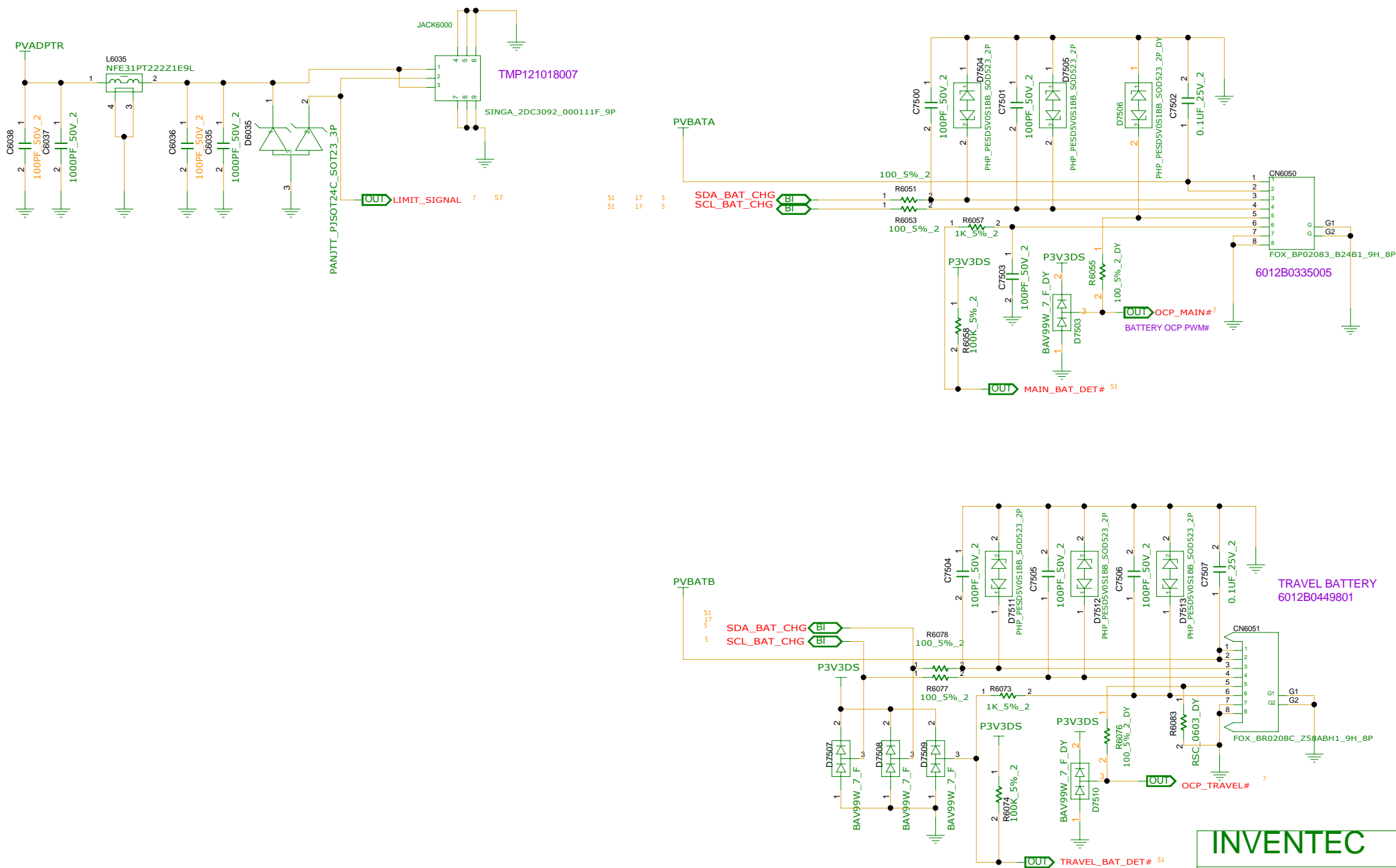
C

B

B

A

A

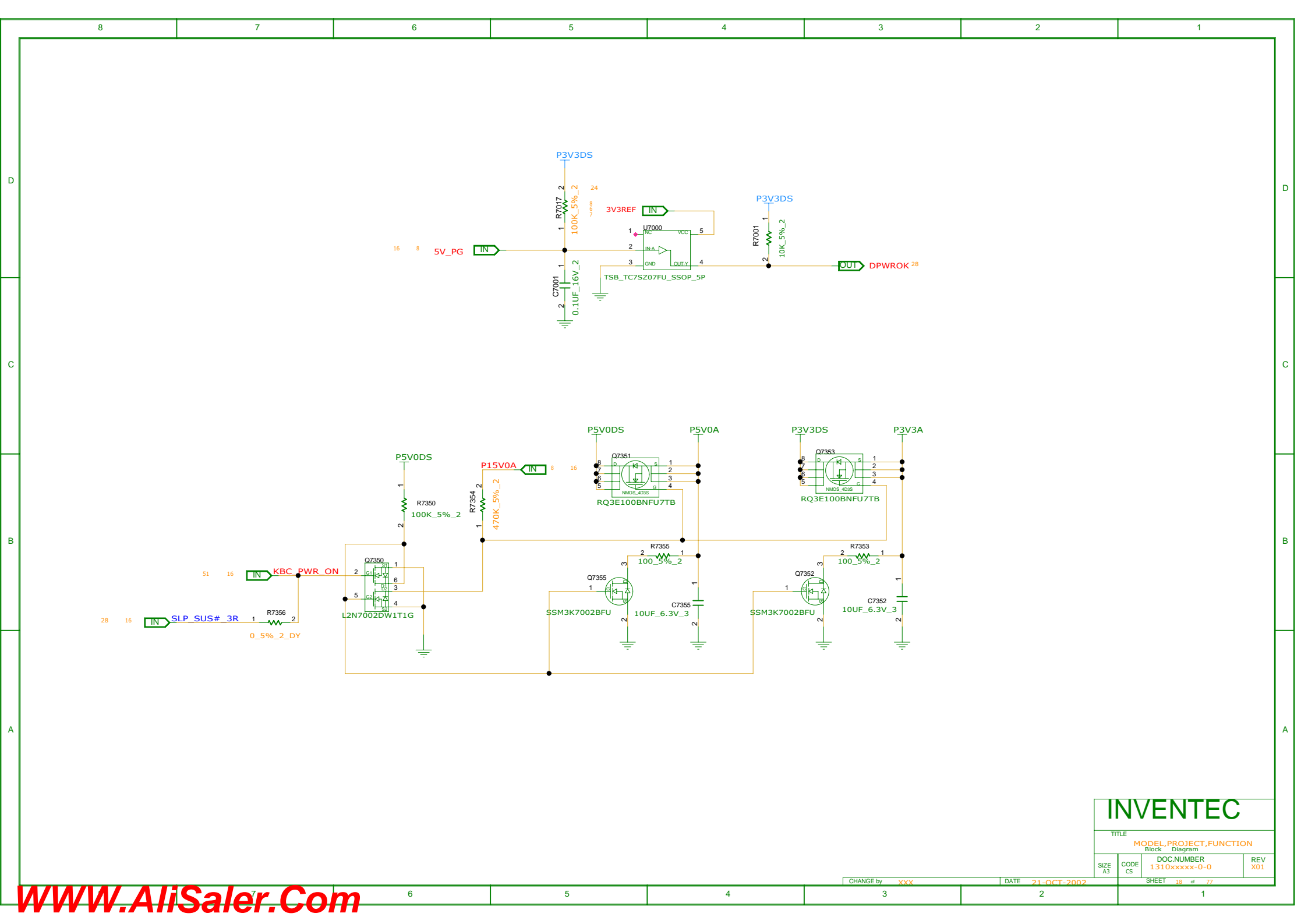
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TITLE

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

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INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002

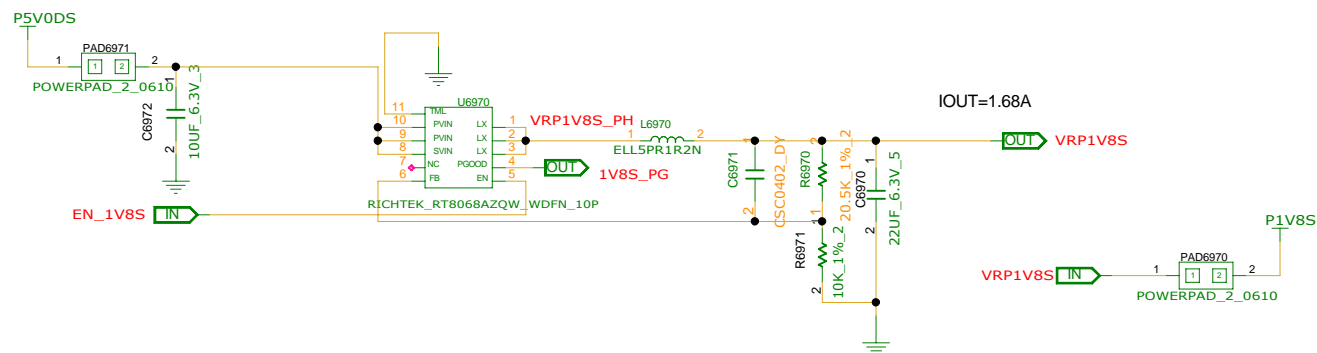
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	8	7	6	5	4	3	2	1
D								
C								
B								
A								

EMPTY

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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VREF=0.6V
 15K=1.5V
 10K=1.2V
 20.5K=1.83V
 MODE=FLOAT=SKIP MODE
 MODE=VIN=FCCM MODE

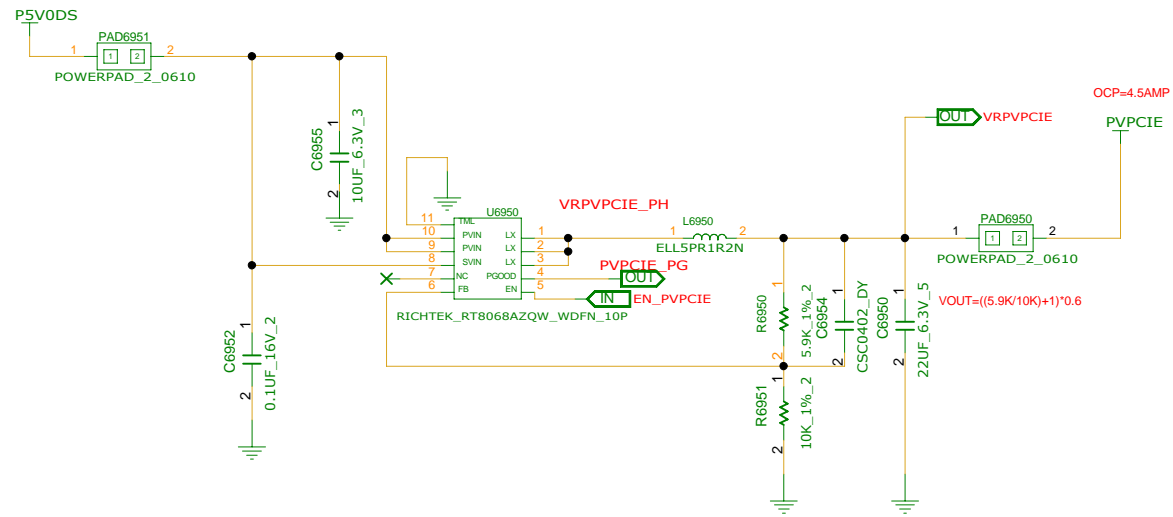
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TITLE
MODEL,PROJECT,FUNCTION

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

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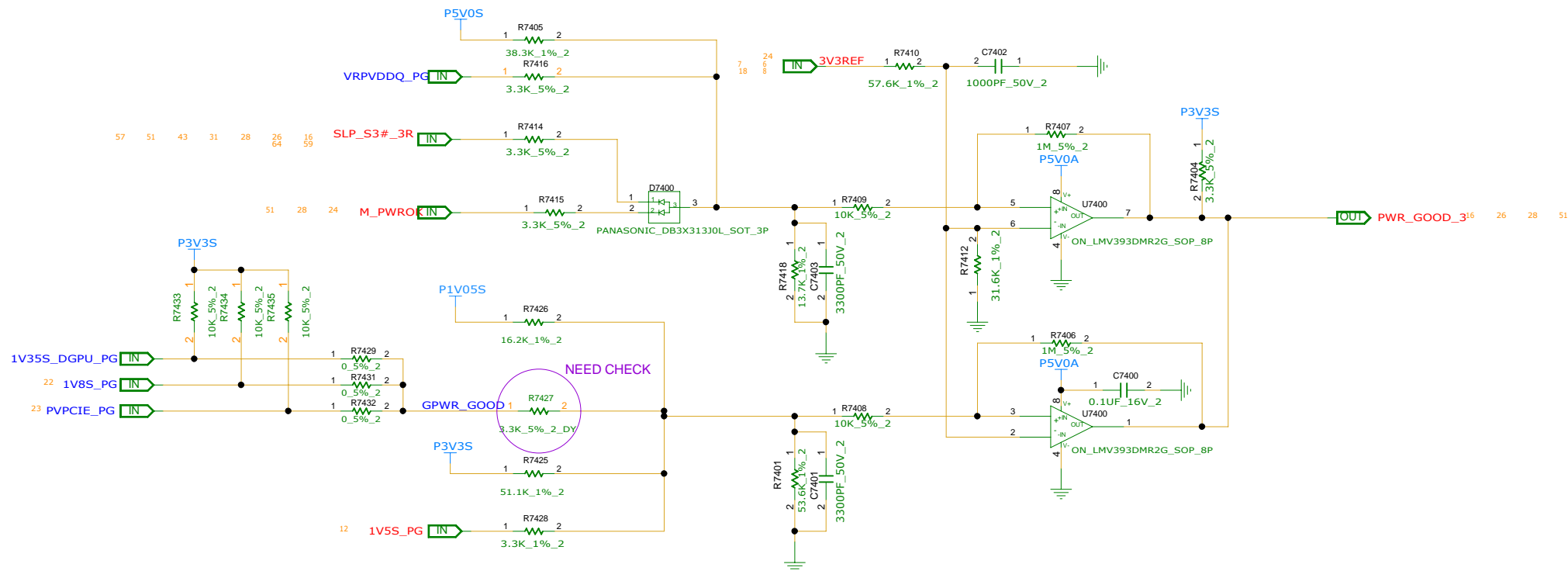
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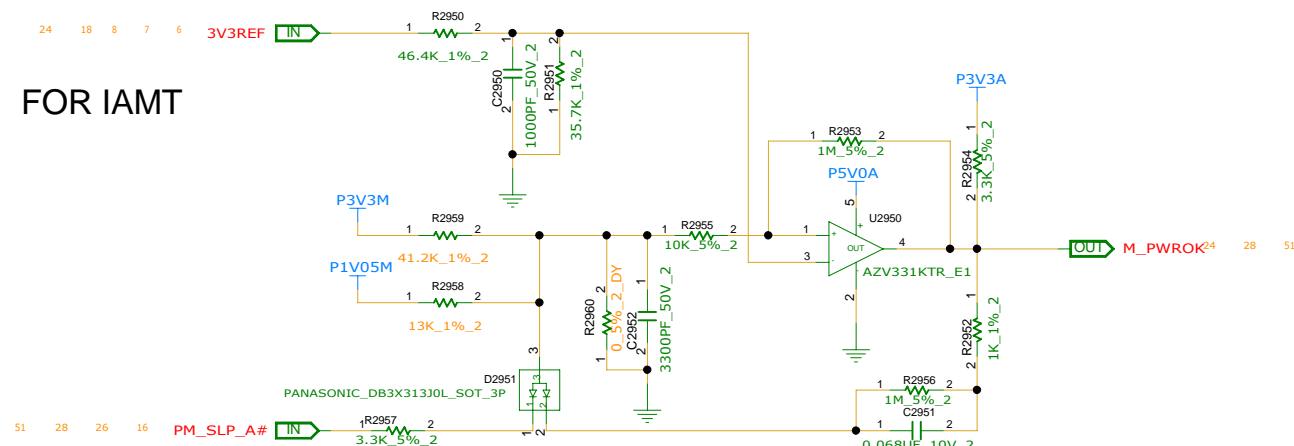
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MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

REFERENCE NUMER : 7400~7450



FOR IAMT



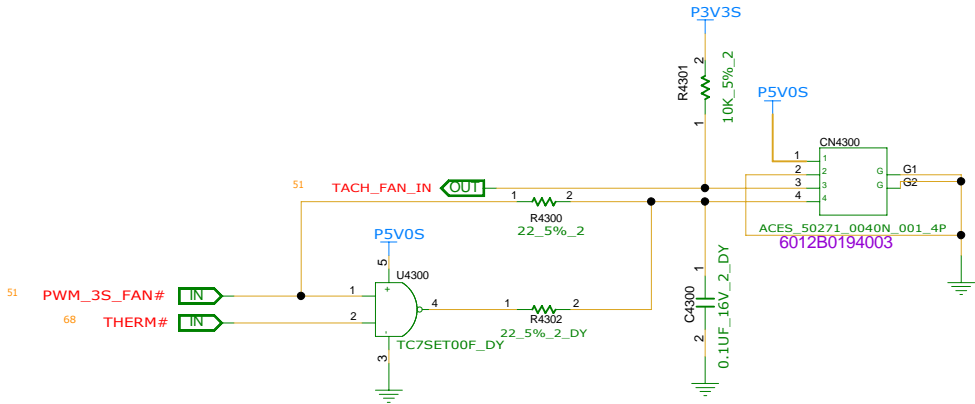
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INVENTEC

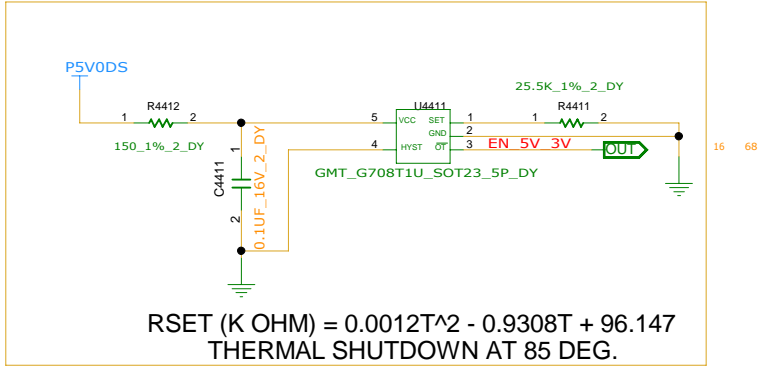
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MODEL PROJECT FUNCTION POWER (SEQUENCE)			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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REFERENCE NUMBER:4400~4349



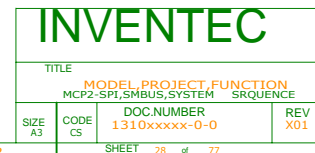
AMBIENT TEMP SENSE
WILL BE NOT USED IN 2013?



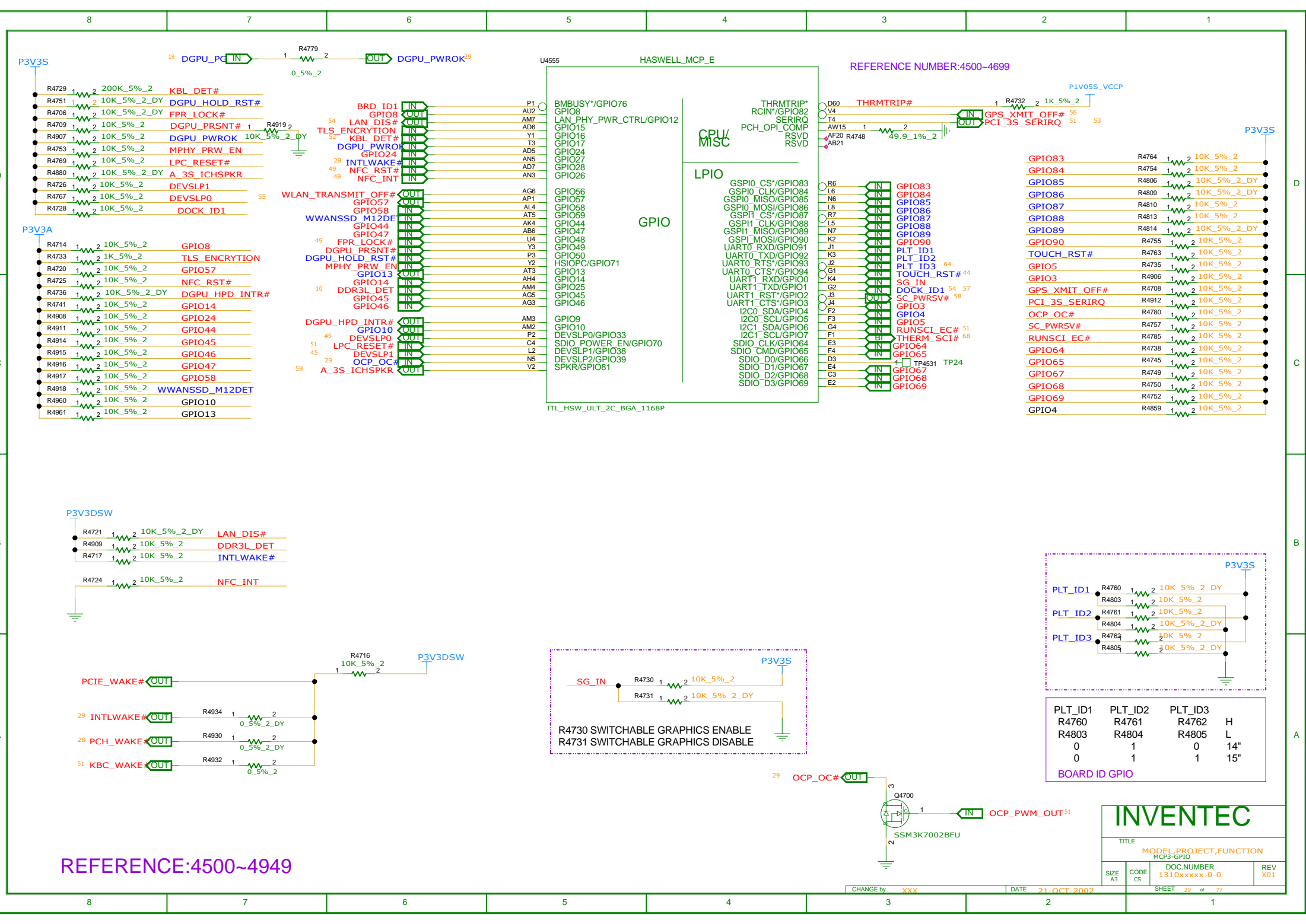
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INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
FAN & THERMAL			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01



CHANGE by	YYY	DATE	31-OCT-2003	SHEET	28	of	77
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D

C

B

A

D

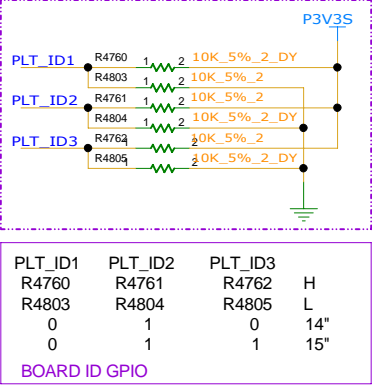
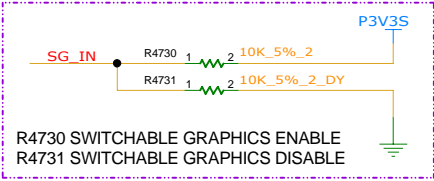
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B

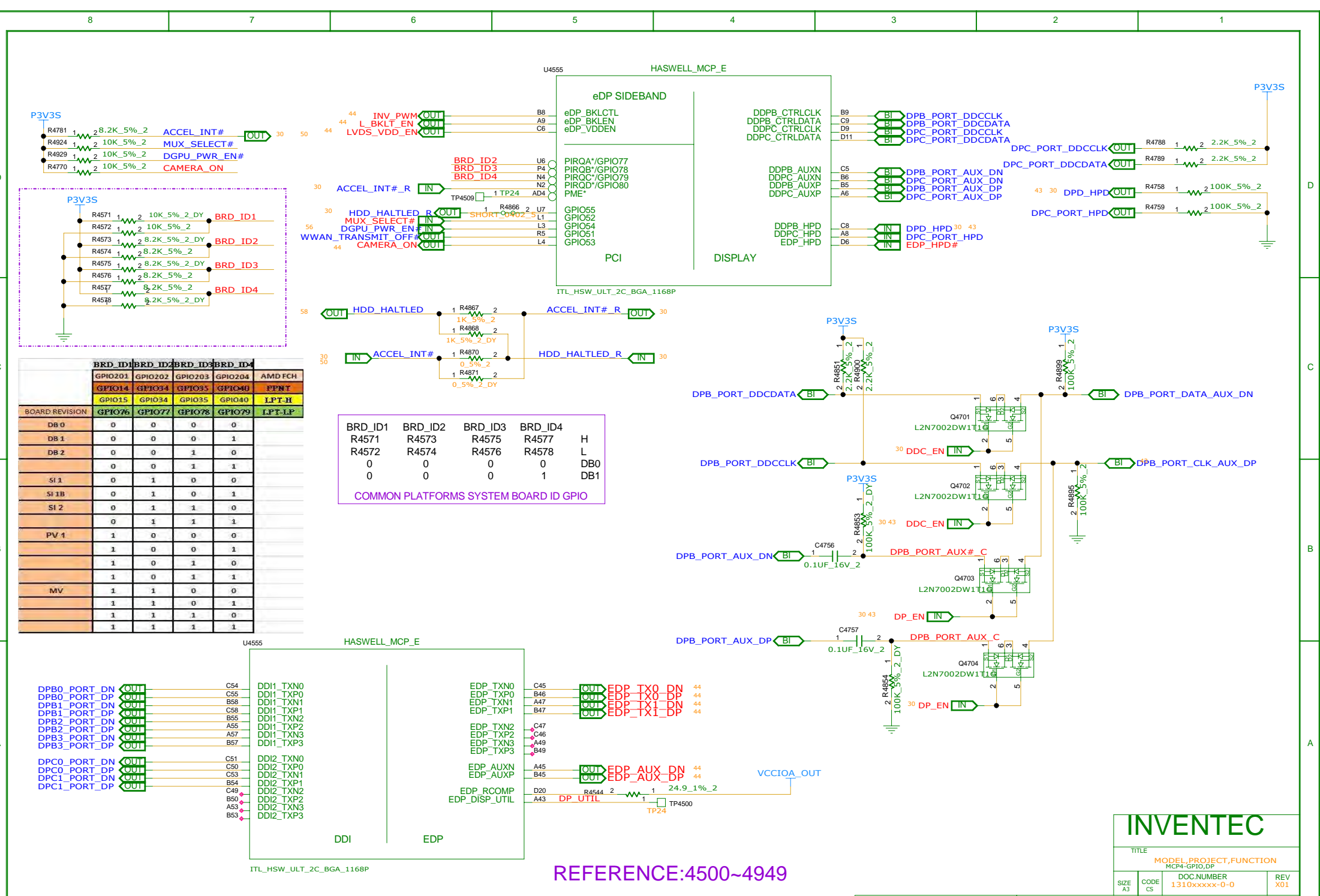
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REFERENCE:4500~4949

REFERENCE NUMBER:4500~4699



INVENTEC			
TITLE			
MODEL PROJECT, FUNCTION			
MCP3-GPIO			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01



BOARD REVISION	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB 0	0	0	0	0	0
DB 1	0	0	0	0	1
DB 2	0	0	1	0	0
SI 1	0	0	1	0	0
SI 1B	0	1	0	1	1
SI 2	0	1	1	0	0
PV 1	0	1	1	1	1
	1	0	0	1	0
	1	0	1	0	0
	1	0	1	1	1
	1	1	0	0	1
	1	1	0	1	0
	1	1	1	0	0
	1	1	1	1	1

BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
R4571	R4573	R4575	R4577	H
R4572	R4574	R4576	R4578	L
0	0	0	0	DB0
0	0	0	1	DB1

COMMON PLATFORMS SYSTEM BOARD ID GPIO

REFERENCE:4500~4949

INVENTEC

TITLE

MODEL PROJECT,FUNCTION

DOC NUMBER

1310xxxxx-0-0

REV

X01

SIZE

A3

CODE

CS

CHANGE by

XXX

DATE

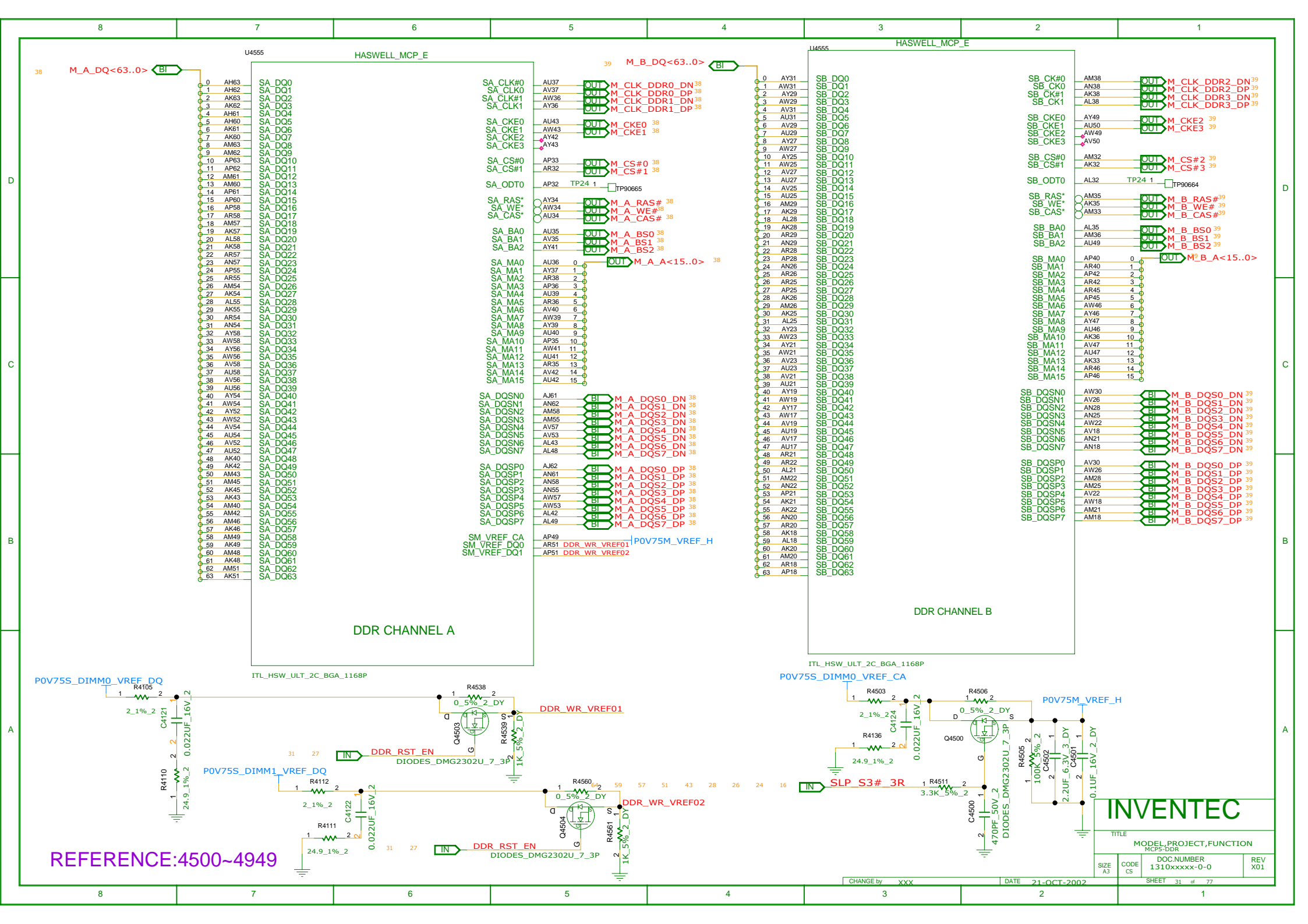
21-OCT-2002

SHEET

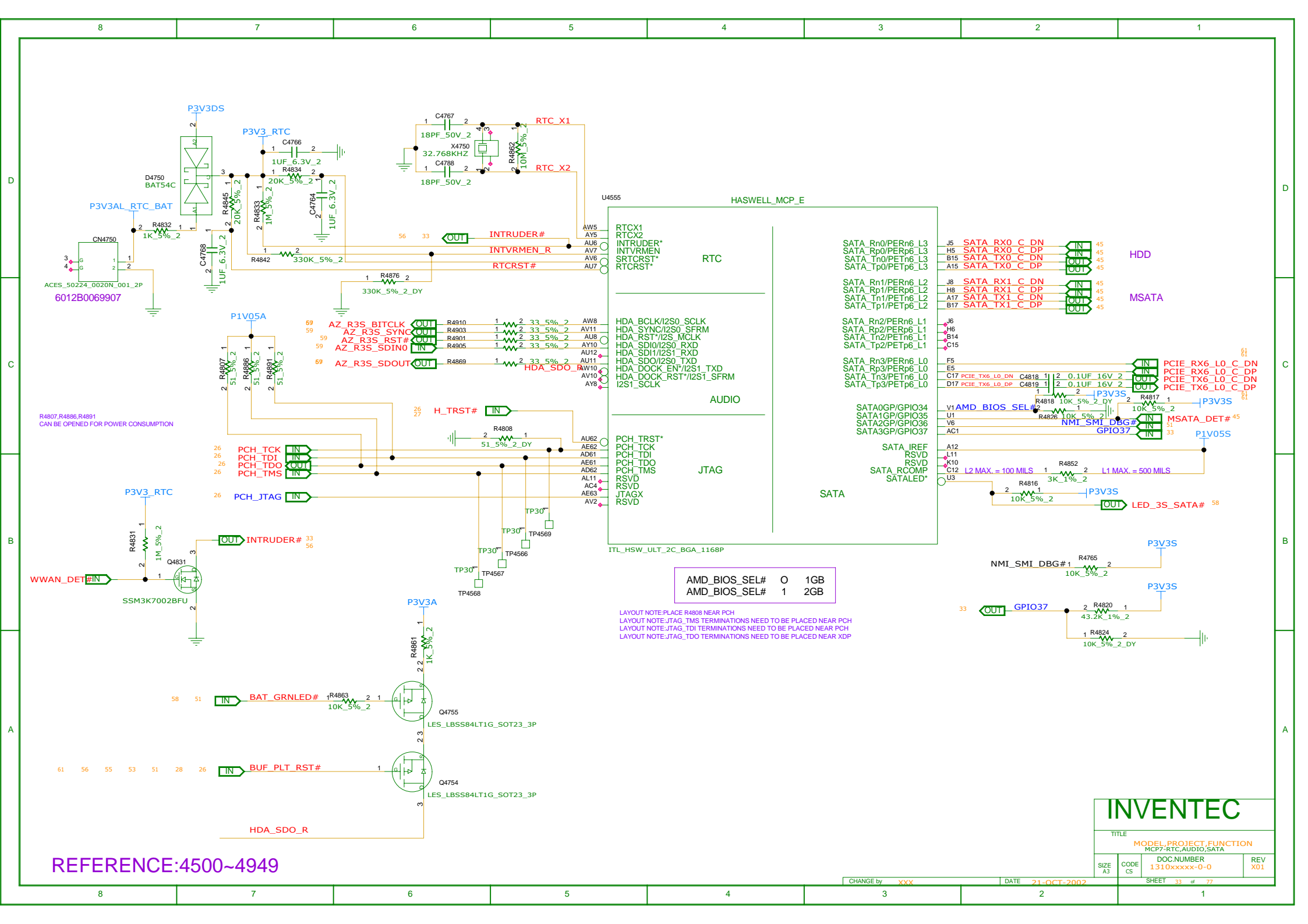
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of

77







REFERENCE:4500~4949

INVENTEC

TITLE

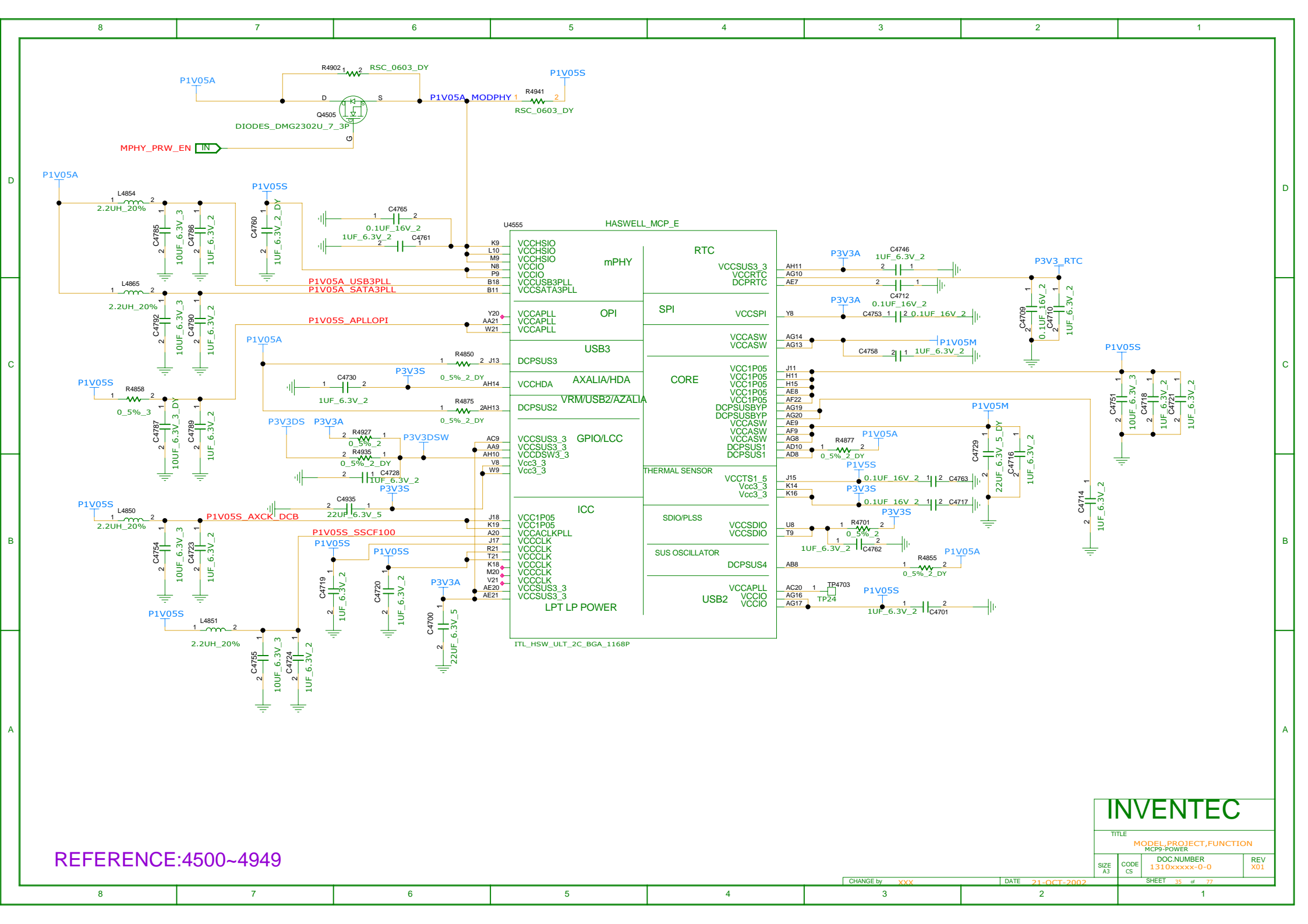
MODEL PROJECT FUNCTION

MCP7-RTC,AUDIO,SATA

SIZE CODE DOC NUMBER REV

A3 CS 1310xxxxx-0-0 X01

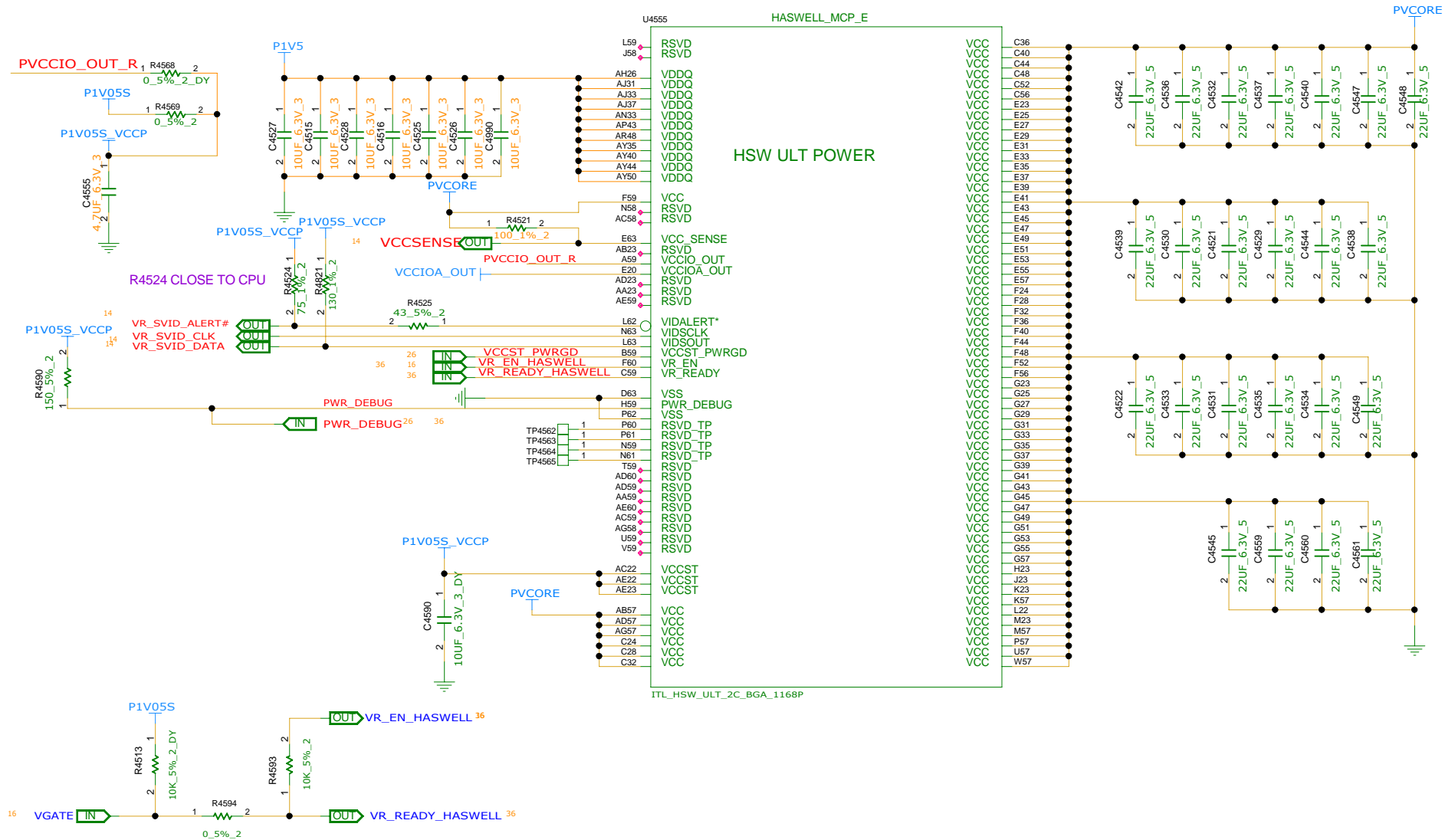
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REFERENCE:4500~4949

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
MCP9-POWER			
SIZE	CODE	DOC NUMBER	REV
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CHANGE by XXX			
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ROUTE VCCSENSE WITH 27.4OHM IMPEDANCE



REFERENCE:4500~4949

INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
MCP10-POWER			
SIZE	CODE	DOC NUMBER	REV
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RESERVED

INVENTEC

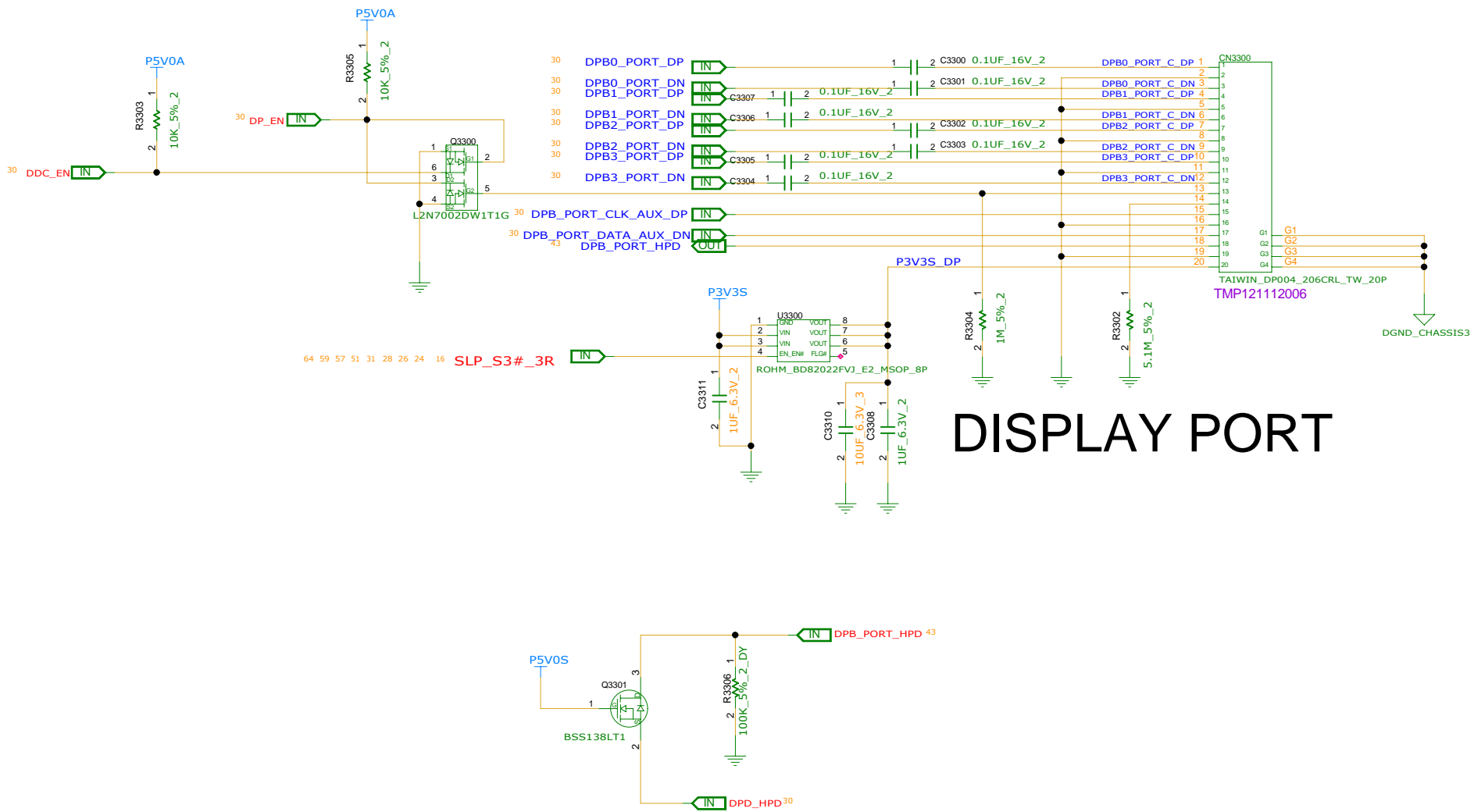
TITLE			
MODEL PROJECT FUNCTION DPB DEMUX1 TO DP			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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RESERVED

INVENTEC

TITLE			
MODEL PROJECT FUNCTION DPC DEMUX2 TO VGA			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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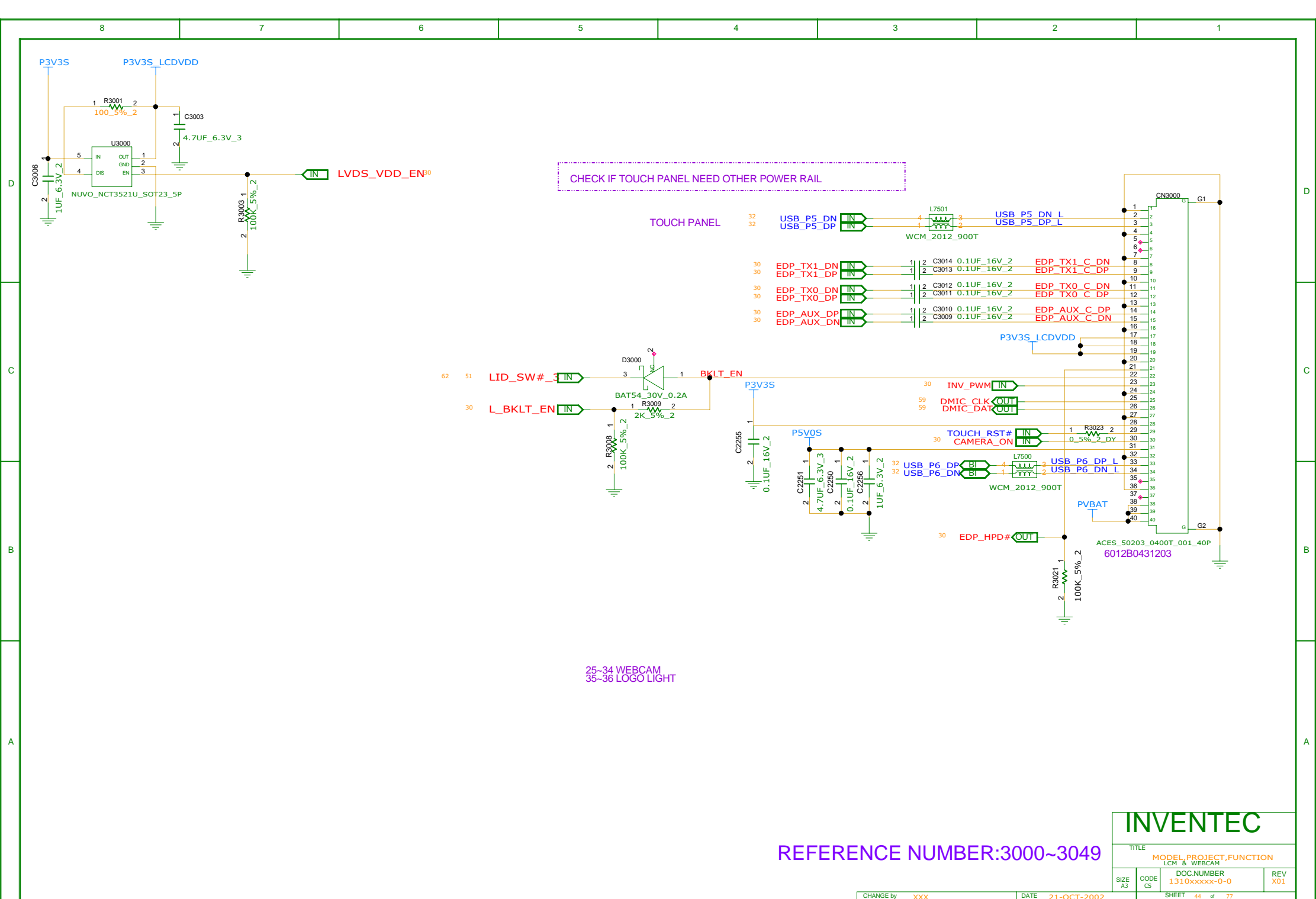




DISPLAY PORT

REFERENCE NUMBER:3300~3399

INVENTEC			
TITLE MODEL PROJECT,FUNCTION CRT & DP			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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REFERENCE NUMBER:1700~1749

REFERENCE NUMBER:1950~1999

M TYPE
6026B0240301
NGFF SSD

SATA HDD CONNECTOR

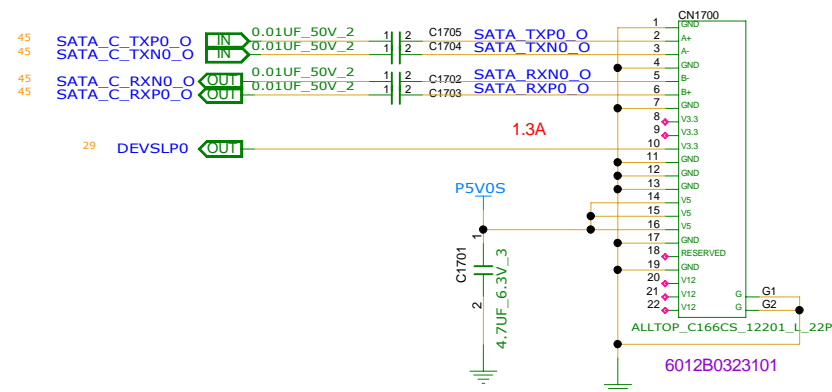
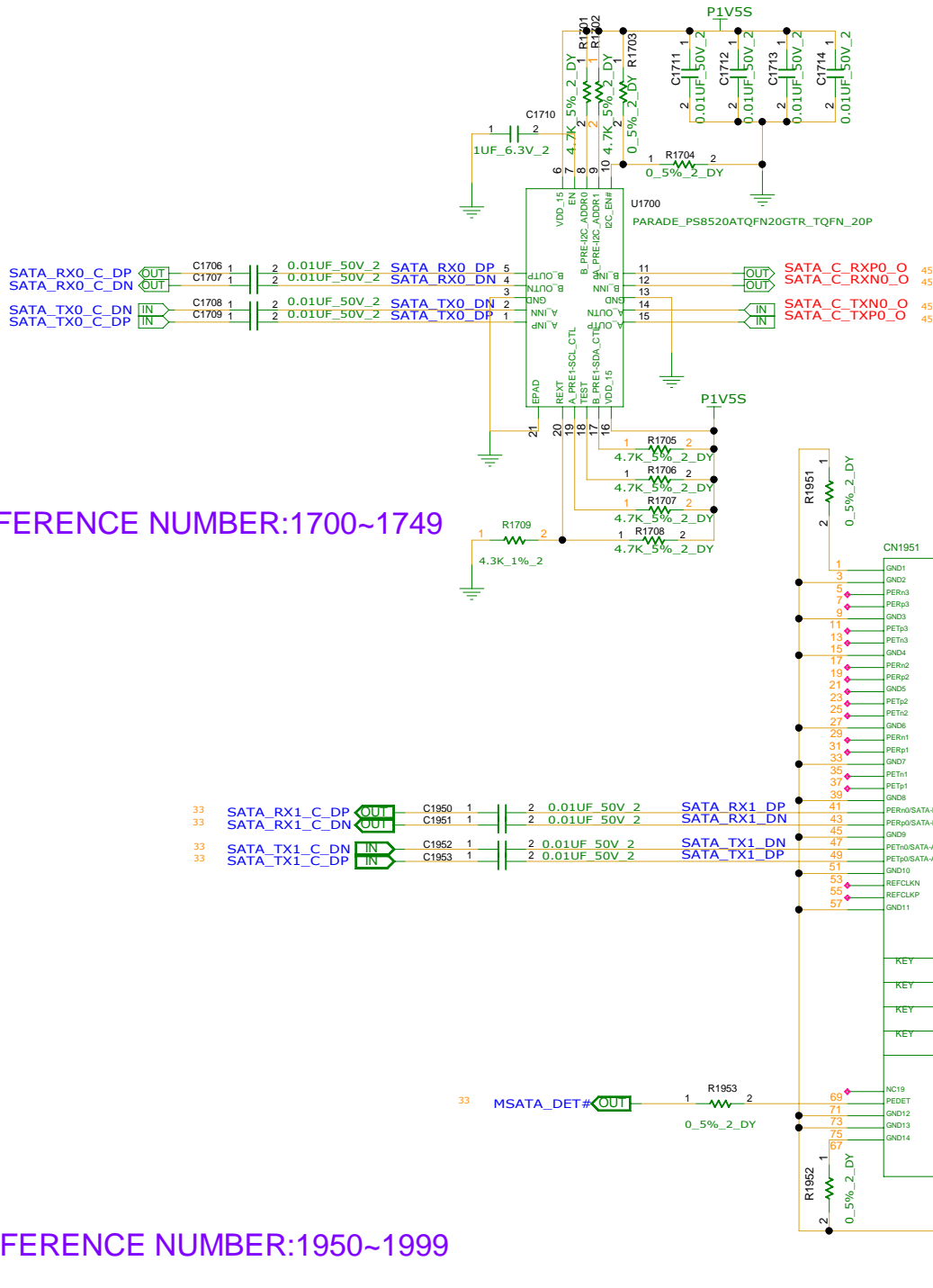
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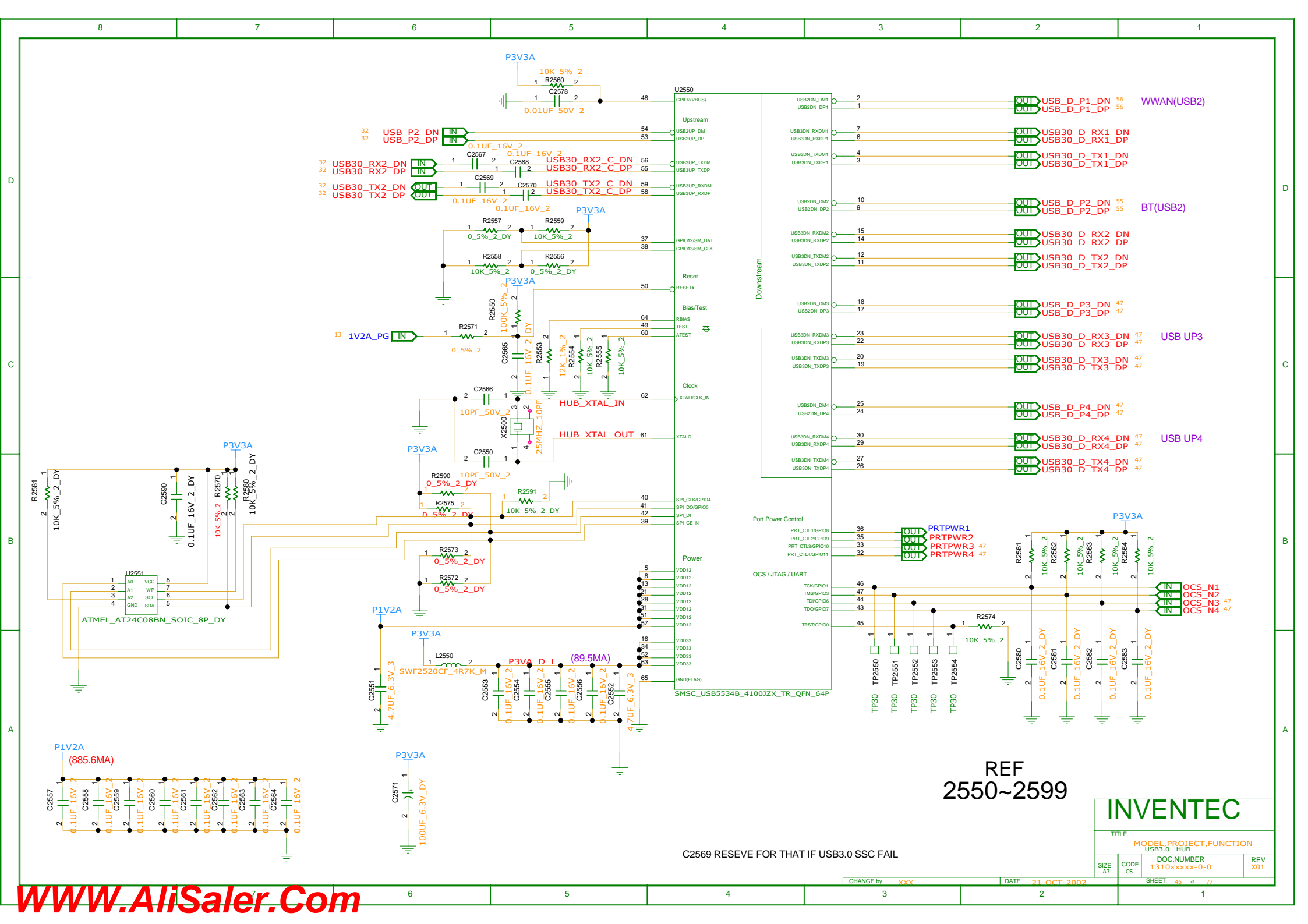
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MODEL,PROJECT,FUNCTION
SATA1_HDD & M-SATA_CONN.

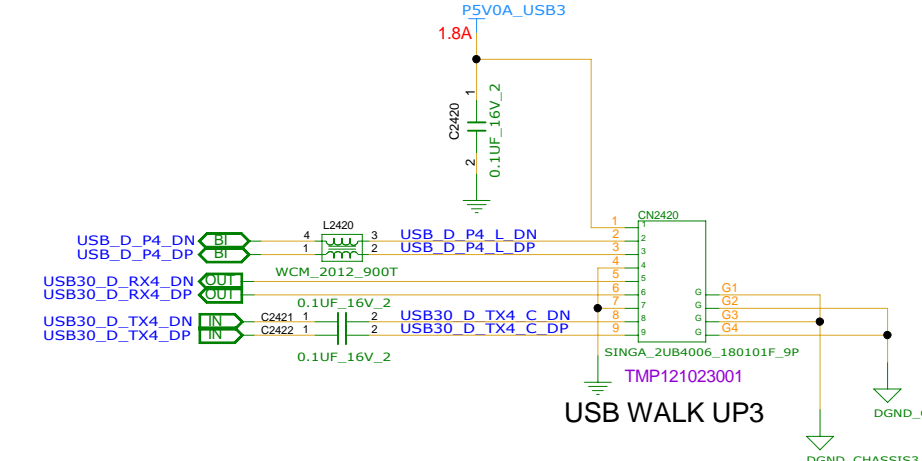
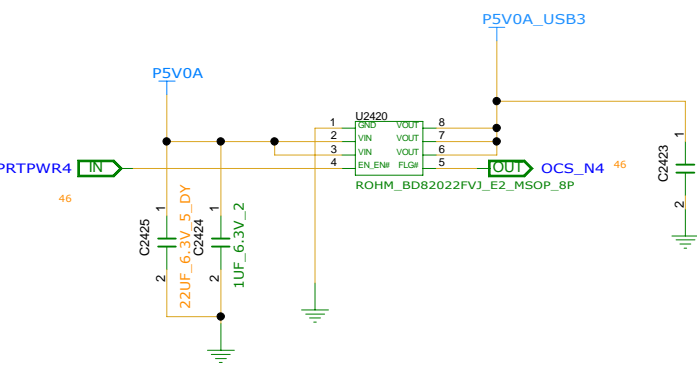
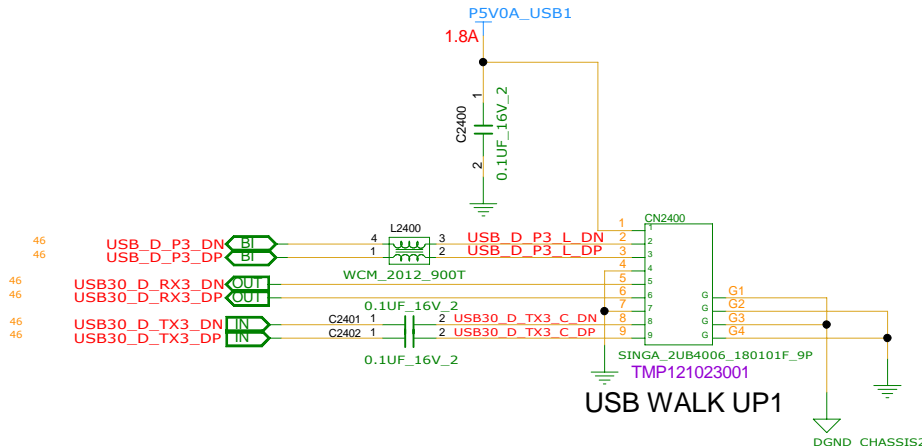
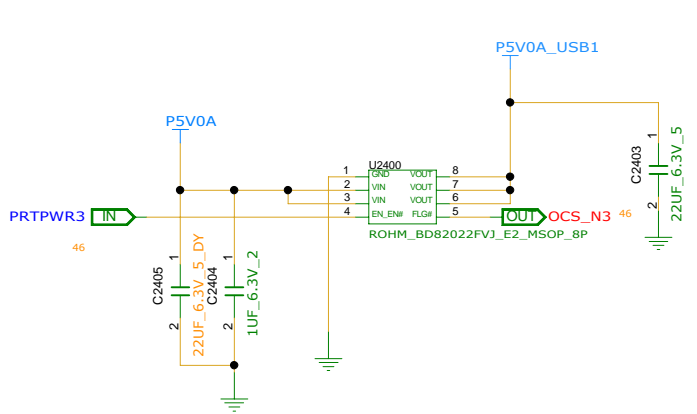
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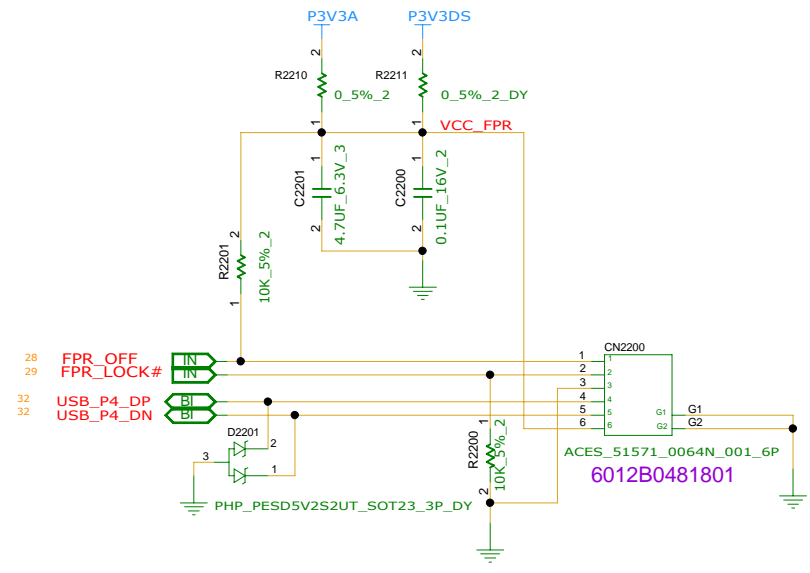




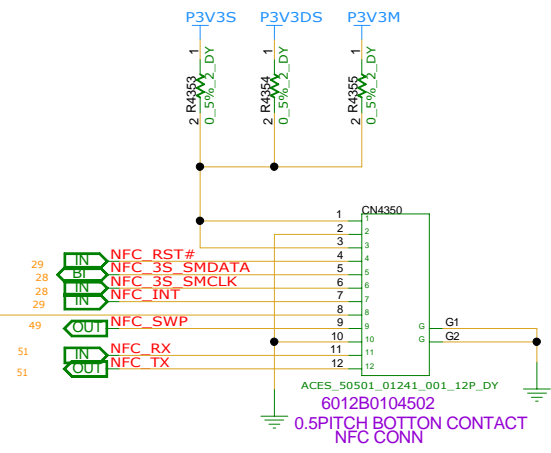


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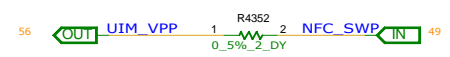
INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
USB & USB CHARGER			
SIZE	CODE	DOC NUMBER	REV
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CHANGE by XXXX			
DATE 21-OCT-2002			
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FINGER PRINT CONN



0.5PITCH BOTTOM CONTACT
NFC CONN

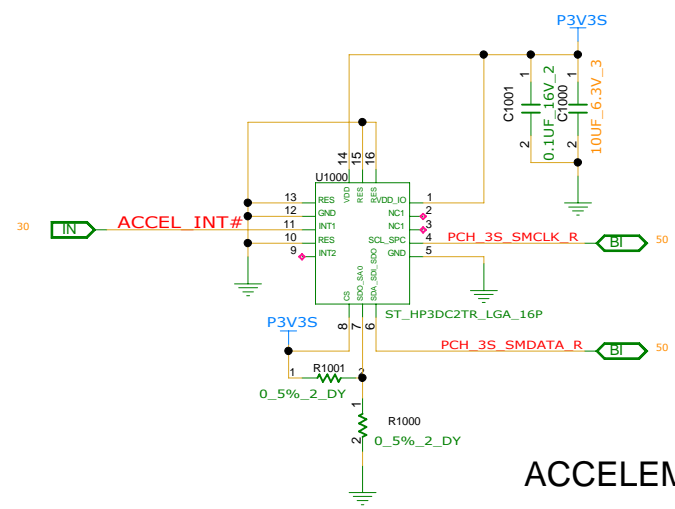


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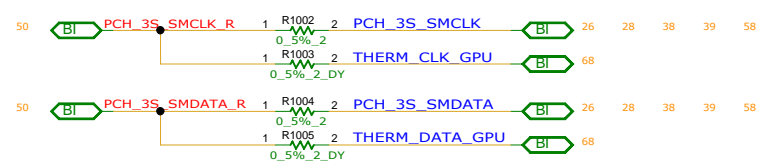
NFC_HI_SEL R4350 R4351
HIGH (UART) INSTALL
LOW (I2C) INSTALL

REFERENCE:4350~4399

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
FINGER PRINTER & NFC			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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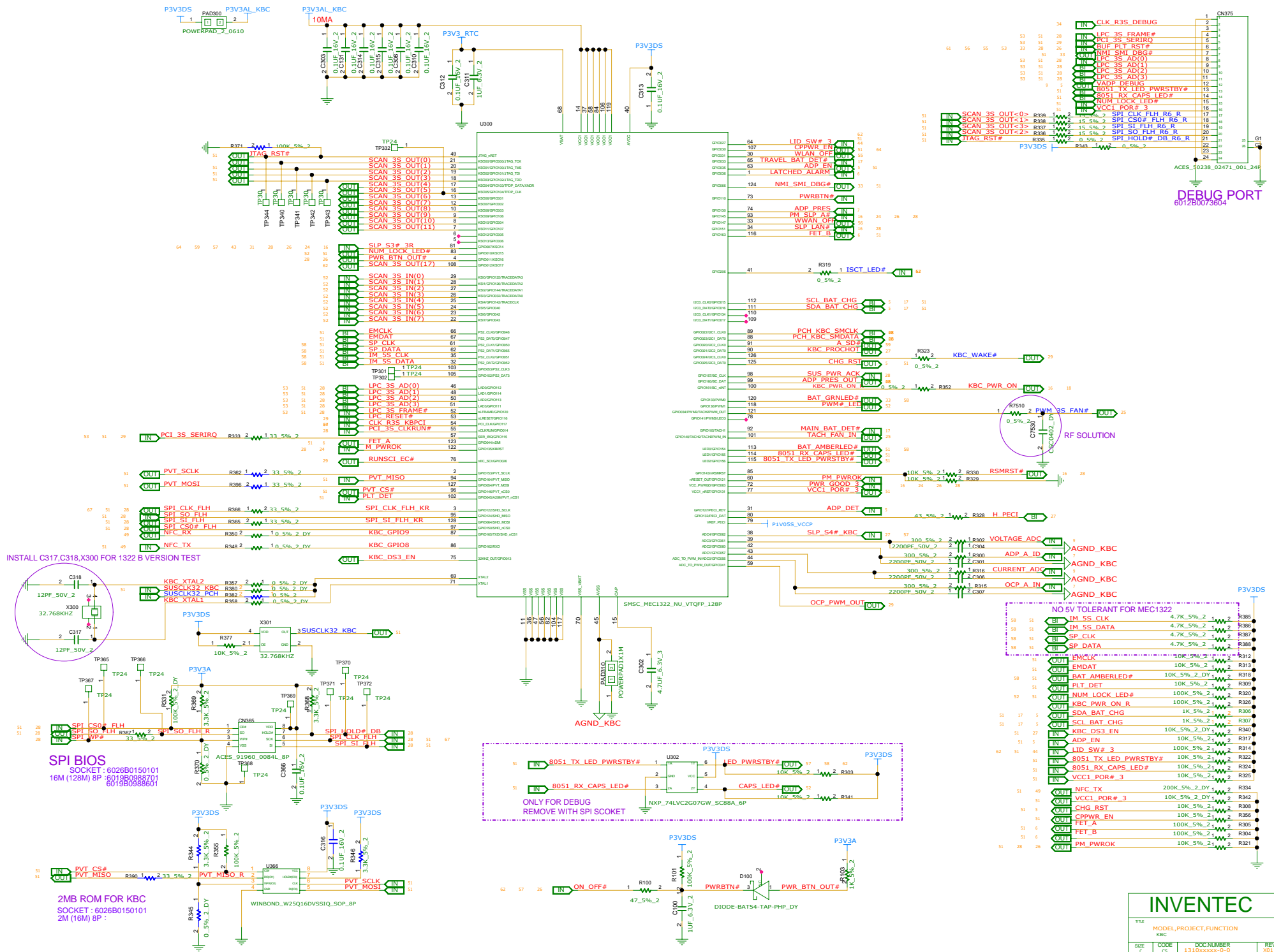
ACCELEMATOR



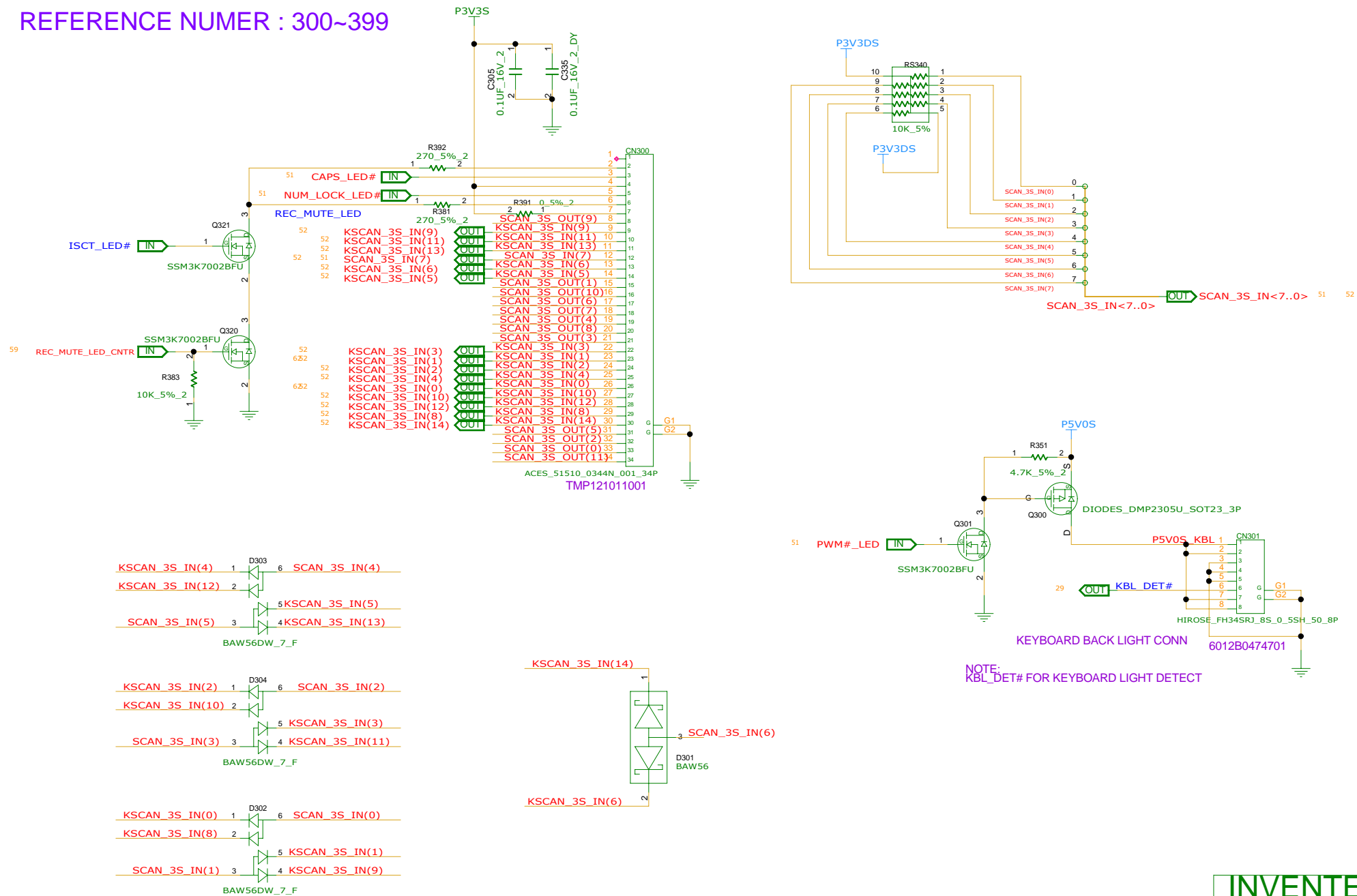
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TITLE			
MODEL PROJECT,FUNCTION			
ACCELEMATOR			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
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REFERENCE NUMER : 1000~1099

REFERENCE NUMBER : 300~399



REFERENCE NUMBER : 300~399



INVENTEC

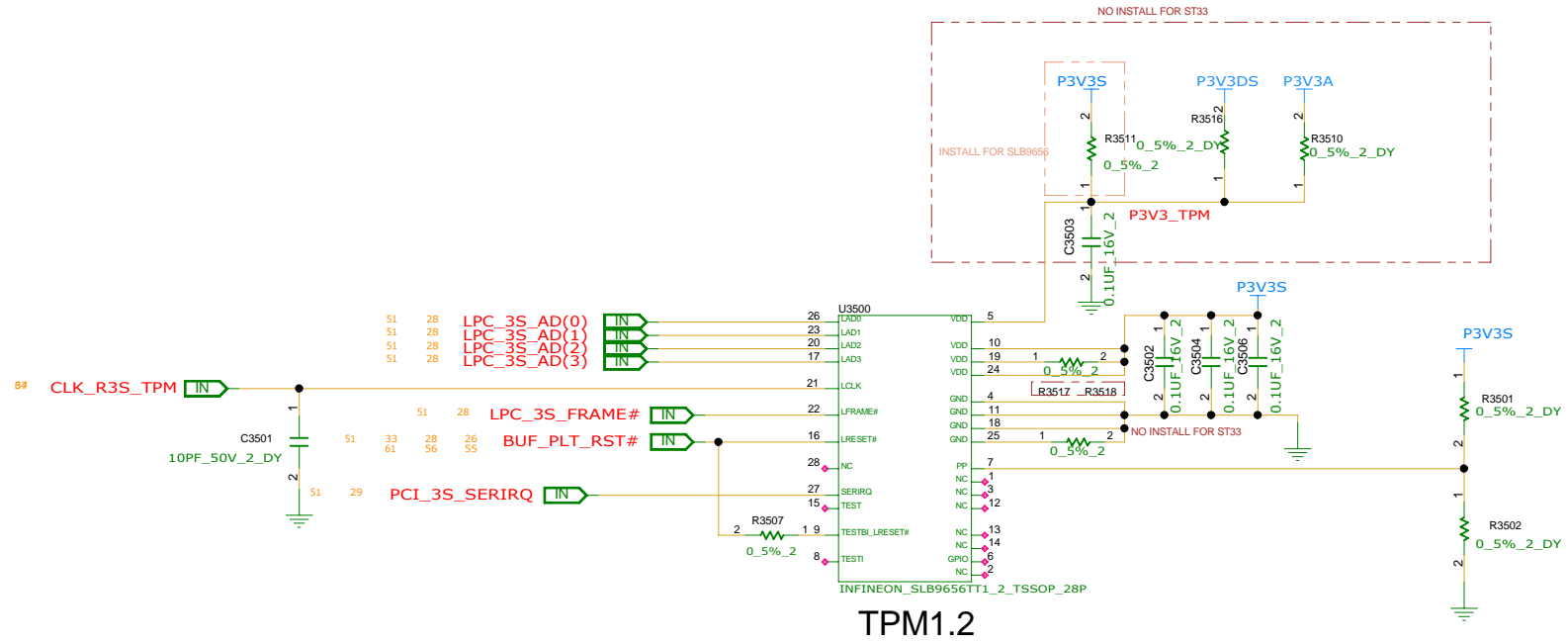
TITLE MODEL PROJECT,FUNCTION

DOC NUMBER 1310xxxxx-0-0

REV X01

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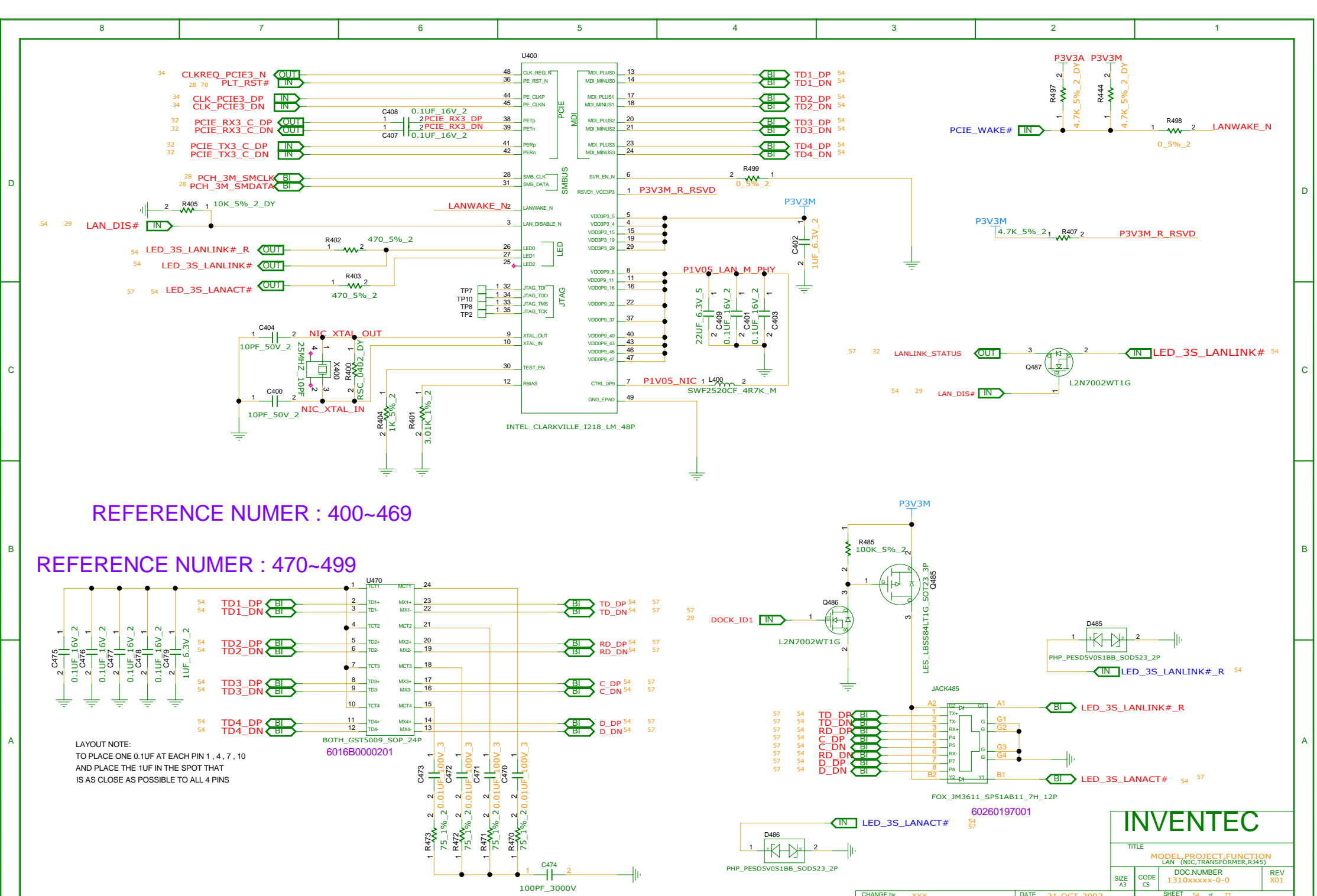


TPM1.2

SLB9656TT1.2		ST33
C3503	INSTALL	OPEN
R3507	INSTALL	OPEN
R3511	INSTALL	OPEN
R3517	INSTALL	OPEN
R3518	INSTALL	OPEN

REFERENCE NUMER : 3500~3549

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION TPM			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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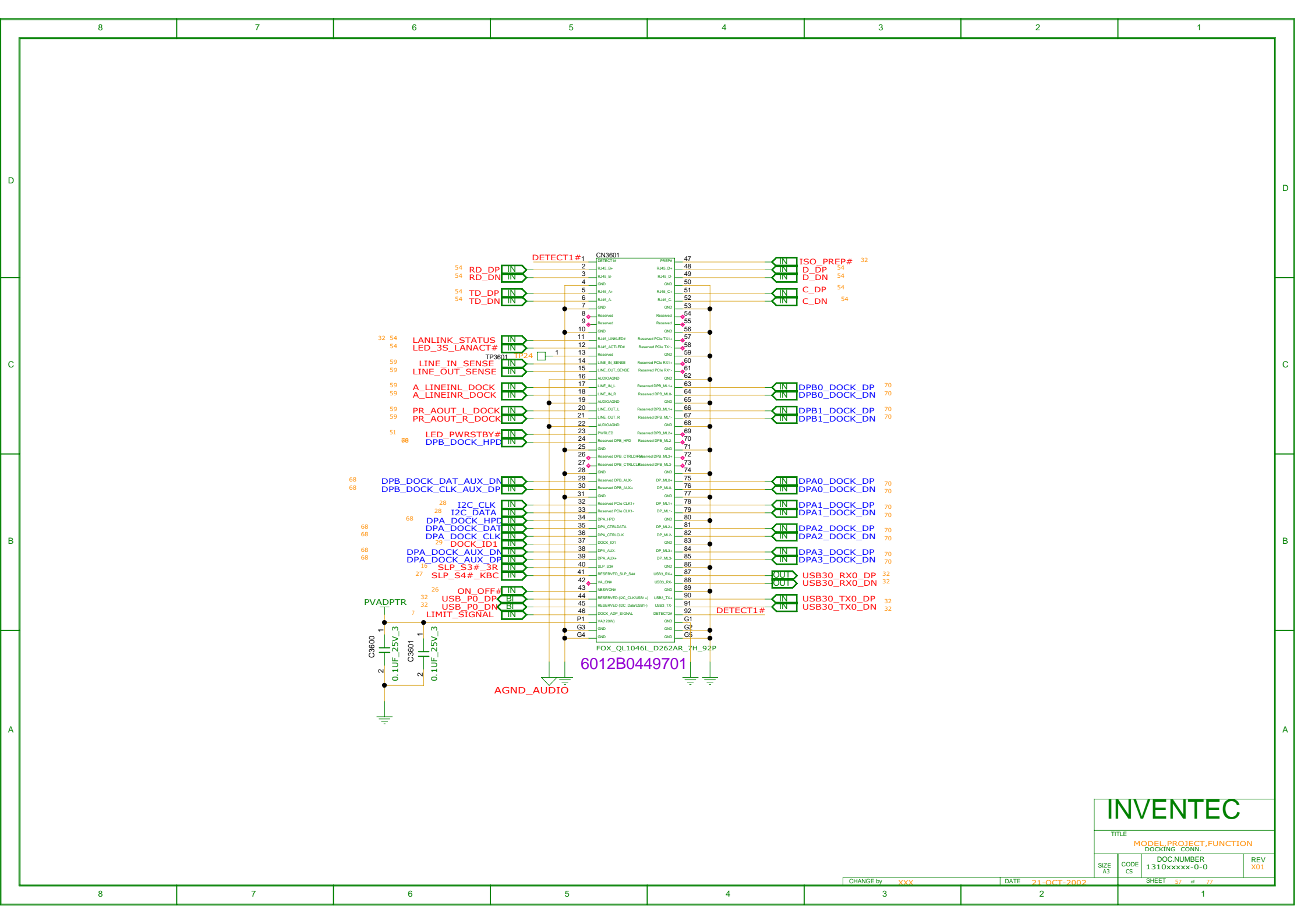
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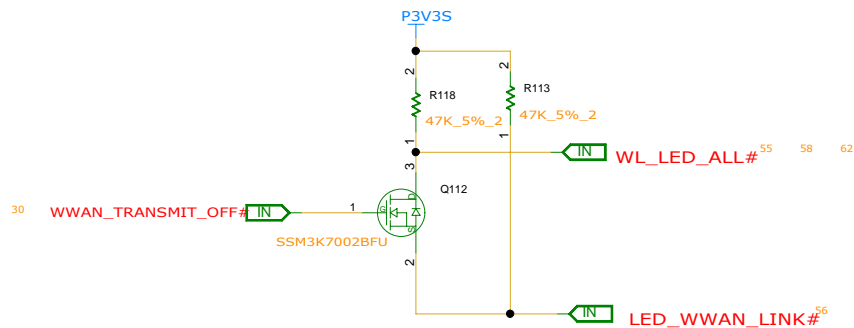
REFERENCE NUMER : 470~499

LAYOUT NOTE:
TO PLACE ONE 0.1UF AT EACH PIN 1, 4, 7, 10
AND PLACE THE 1UF IN THE SPOT THAT
IS AS CLOSE AS POSSIBLE TO ALL 4 PINS

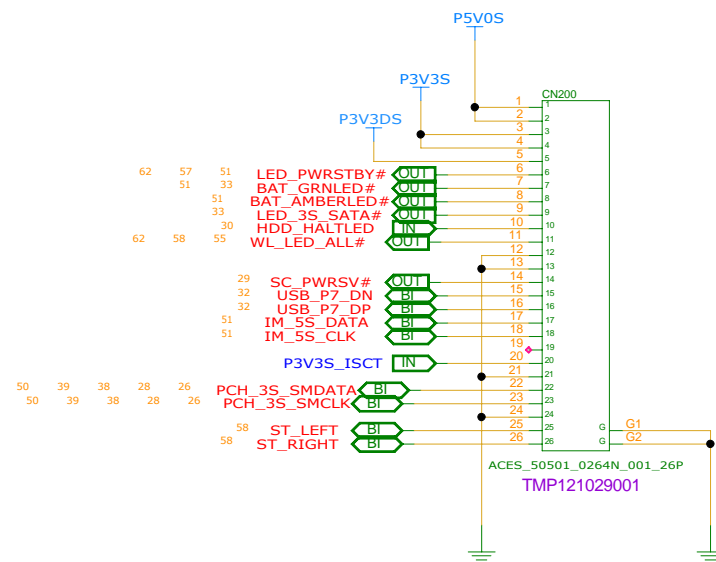
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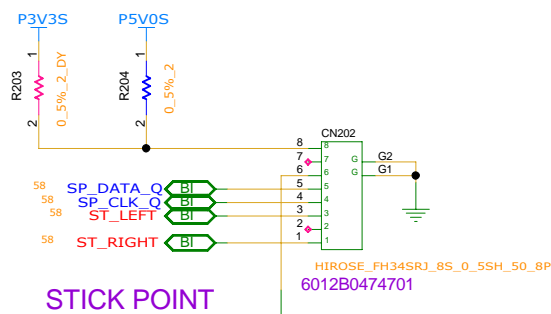




WLAN_WWAN_BLUETOOTH_LED

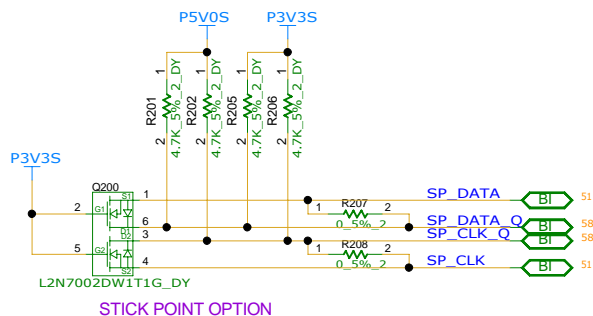


SMART CARD AND TOUCHPAD D/B W TO B CONN



STICK POINT

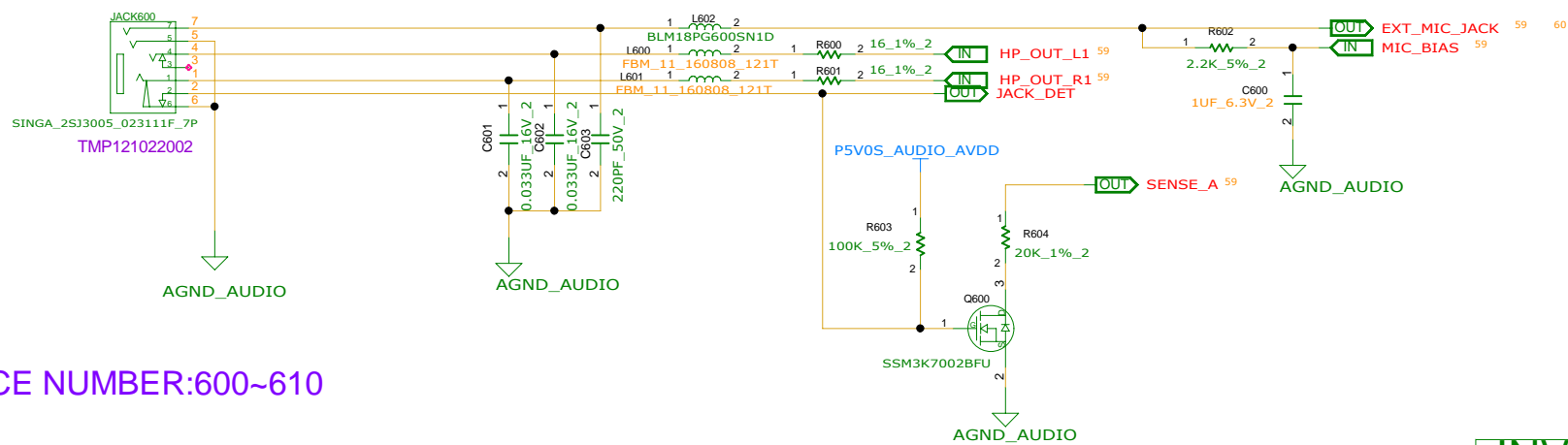
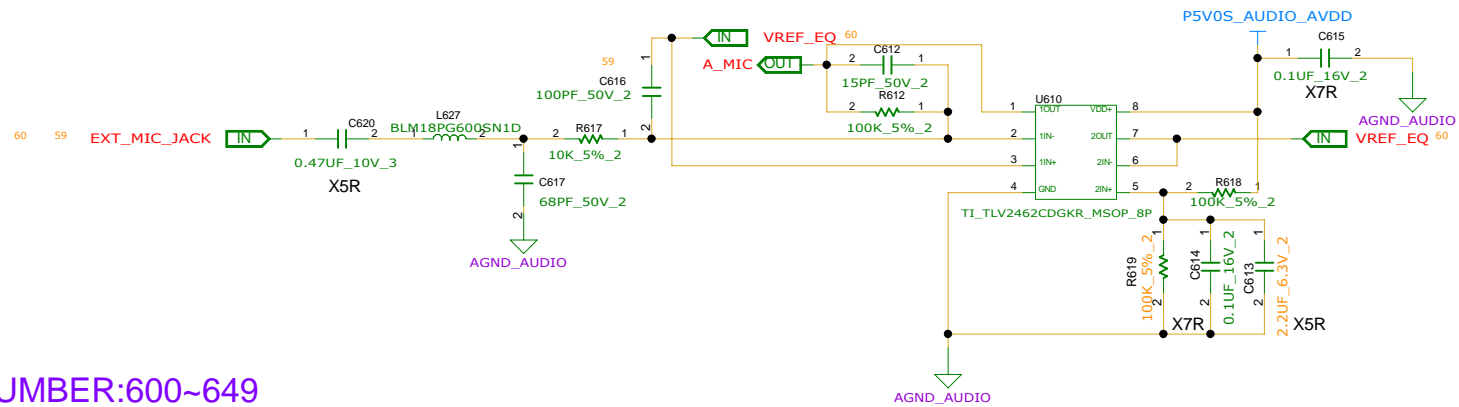
	5V	3.3V
R201	INSTALL	UNINSTALL
R202	INSTALL	UNINSTALL
R203	UNINSTALL	INSTALL
R204	INSTALL	UNINSTALL



STICK POINT OPTION

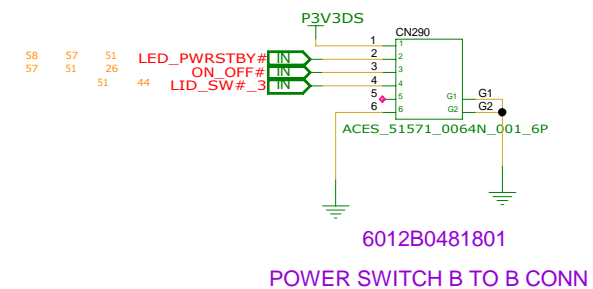
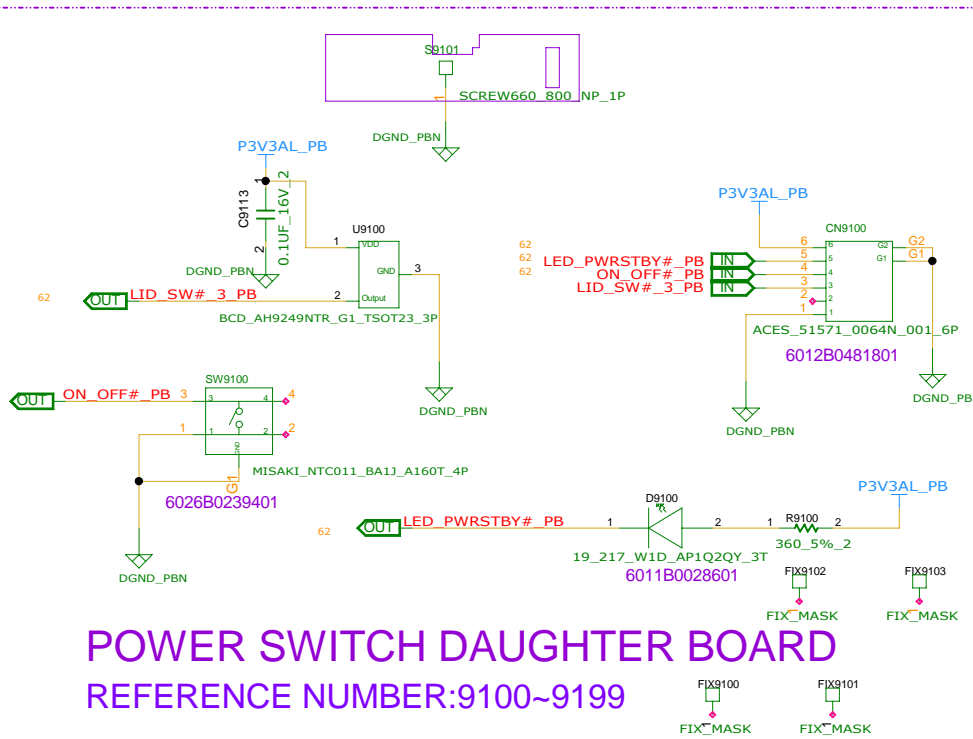
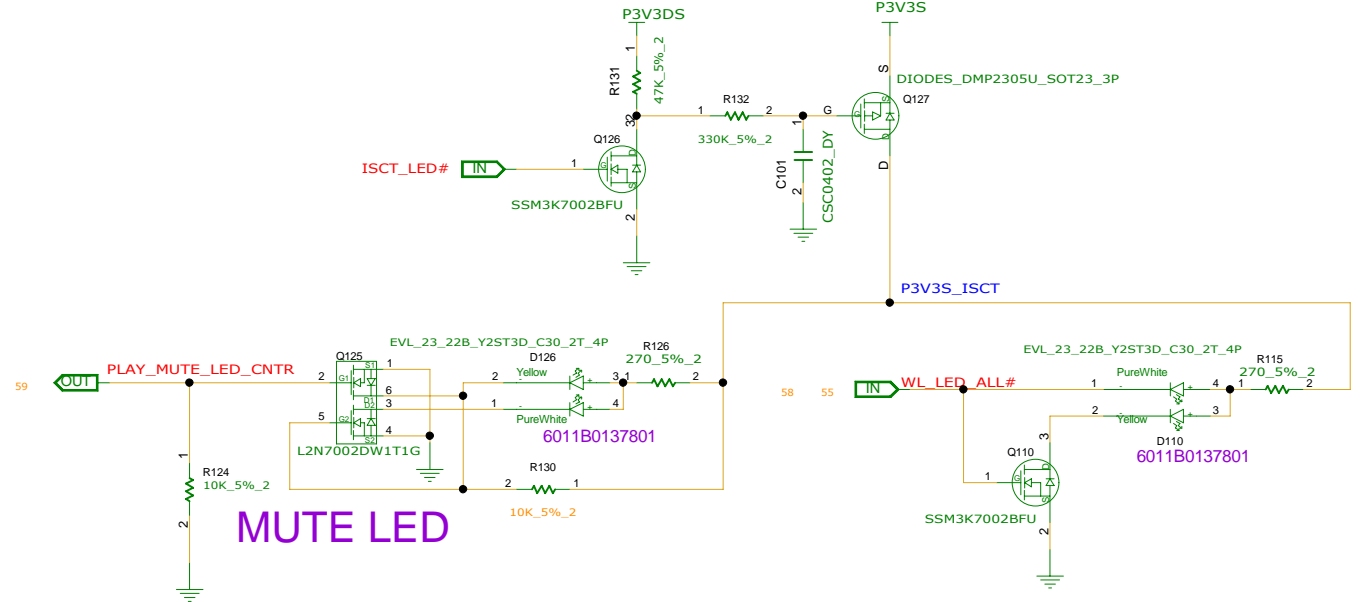
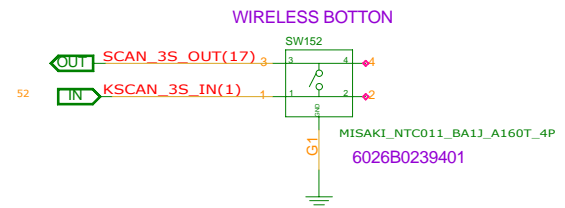
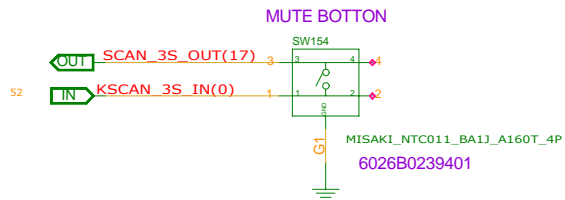
REFERENCE NUMBER:100~199

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
STICK POINT & B2B CNTR			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 58 of 77			



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
EXT. MIC AMP. & AUDIO JACK			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 60 of 77			

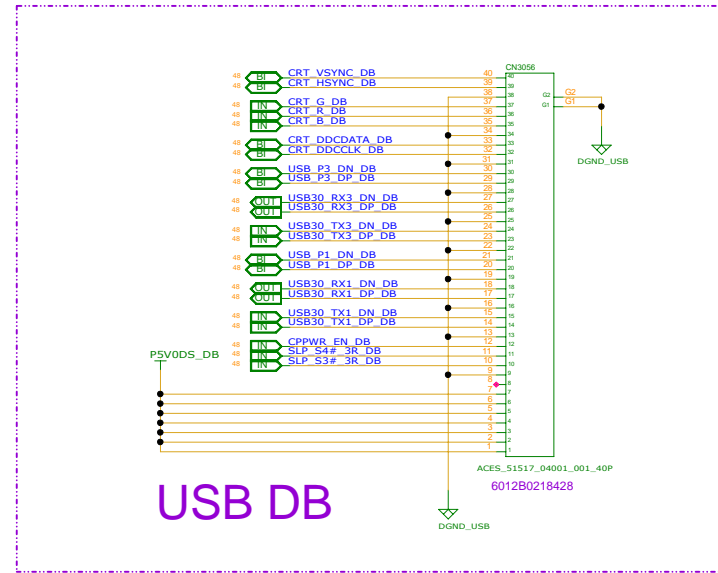
CHANGE by XXX DATE 21-OCT-2002



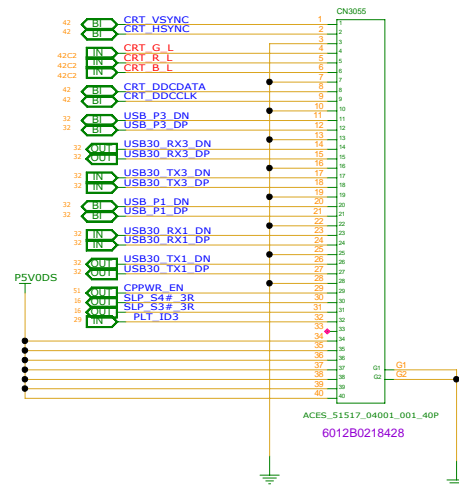
POWER SWITCH DAUGHTER BOARD
REFERENCE NUMBER:9100~9199

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
BUTTON LED			
SIZE A3	CODE C3	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 62 of 77			

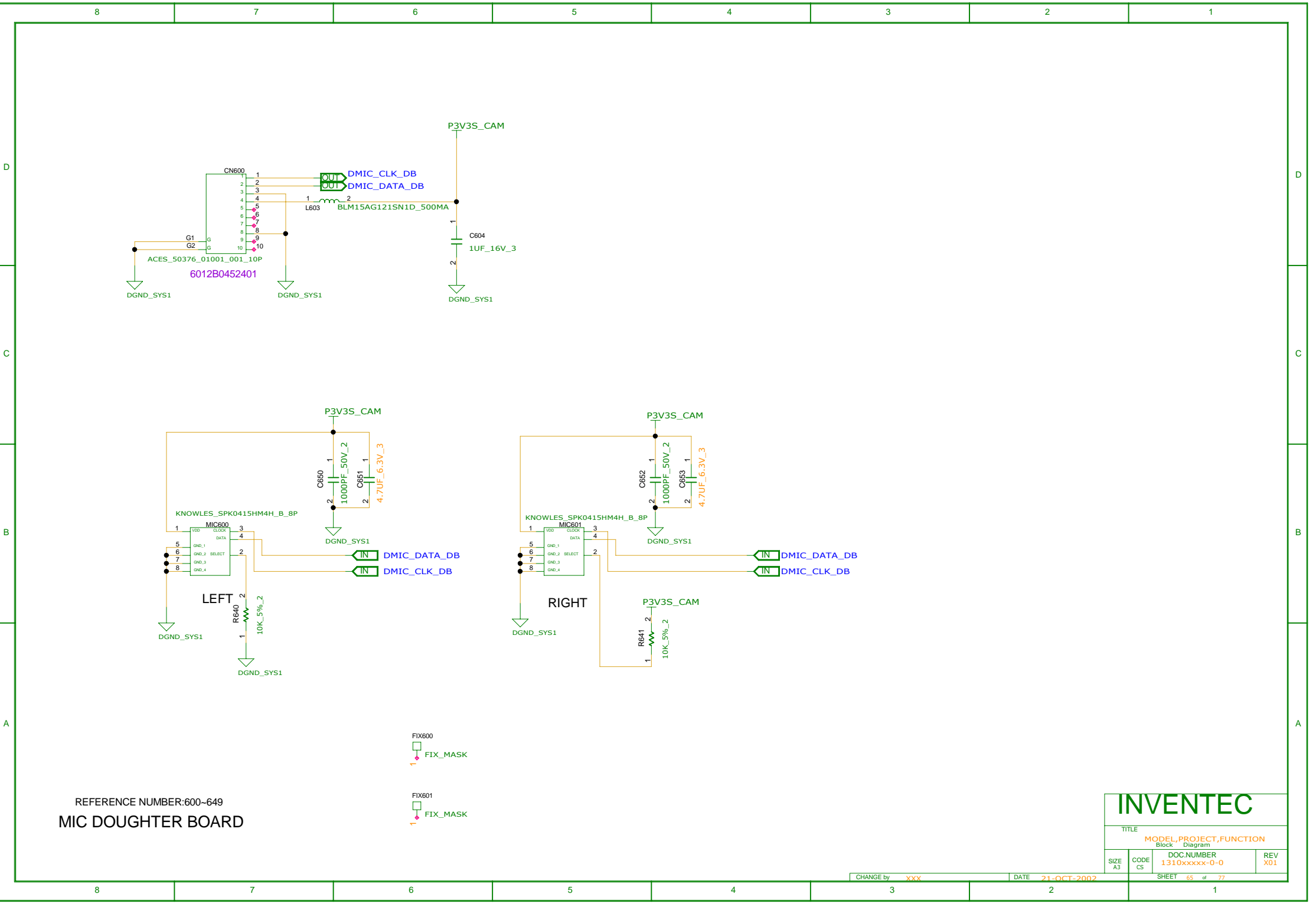
CHANGE by XXX DATE 21-OCT-2002

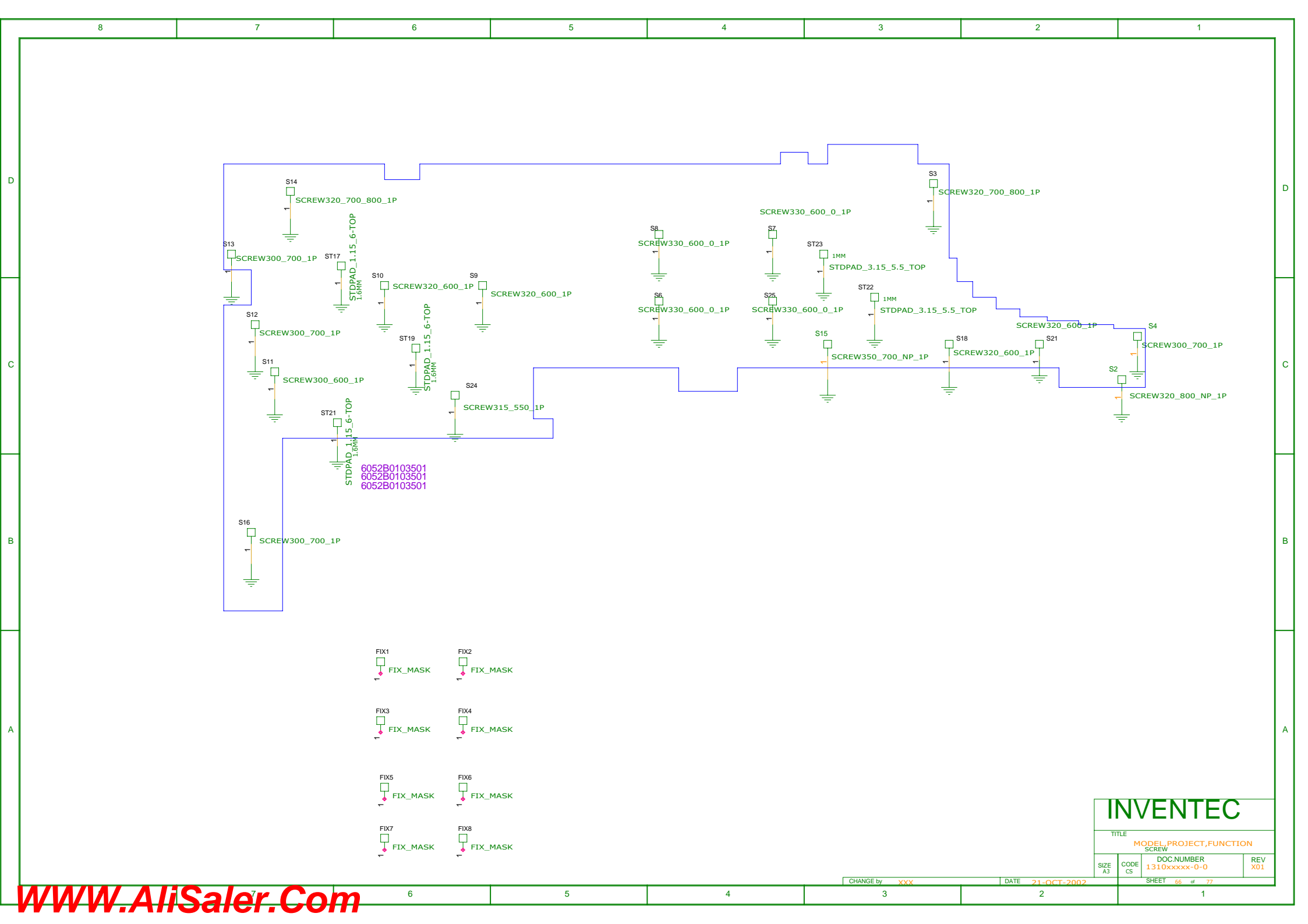


USB DB



INVENTEC				
TITLE				
MODEL,PROJECT,FUNCTION				
RESERVE				
SIZE	CODE	DOC NUMBER	REV	
C	CS	1310XXXX-0-0	201	
CHANGE BY		DATE	SHEET	
XXX		21-OCT-2002	64 of 67	

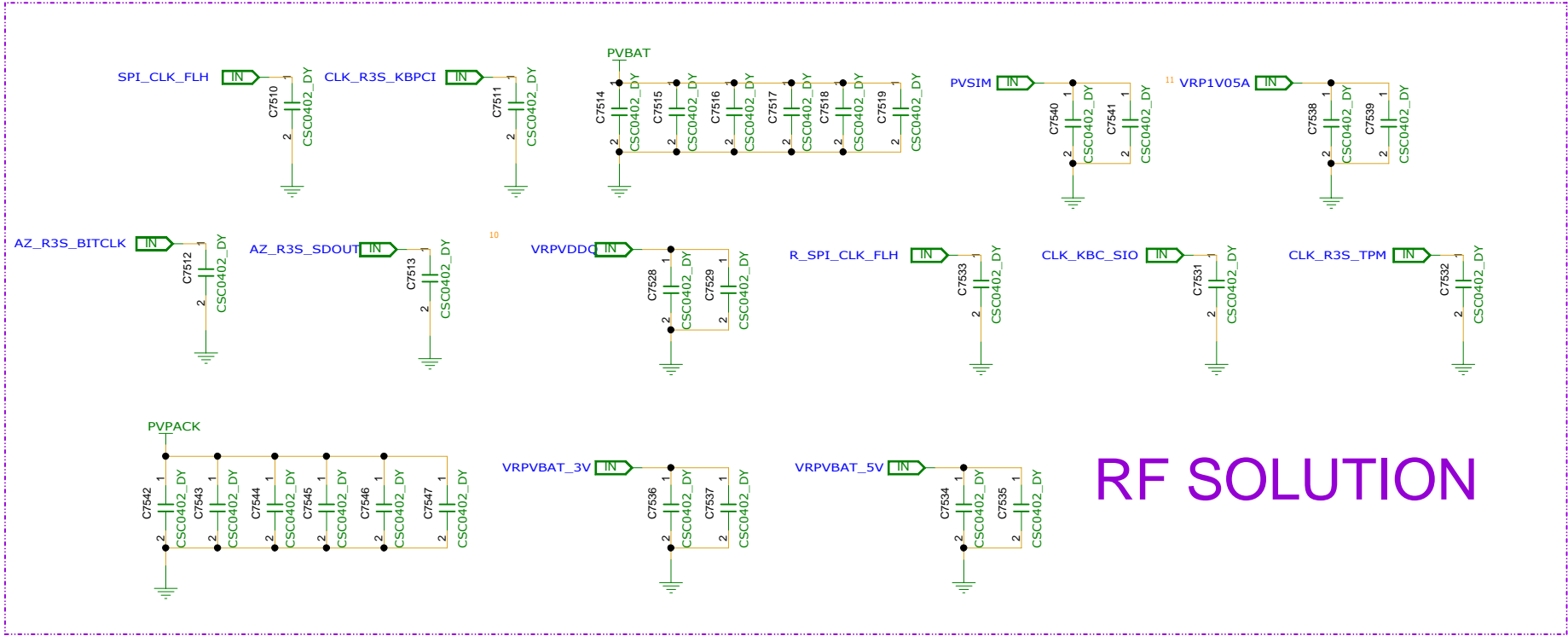




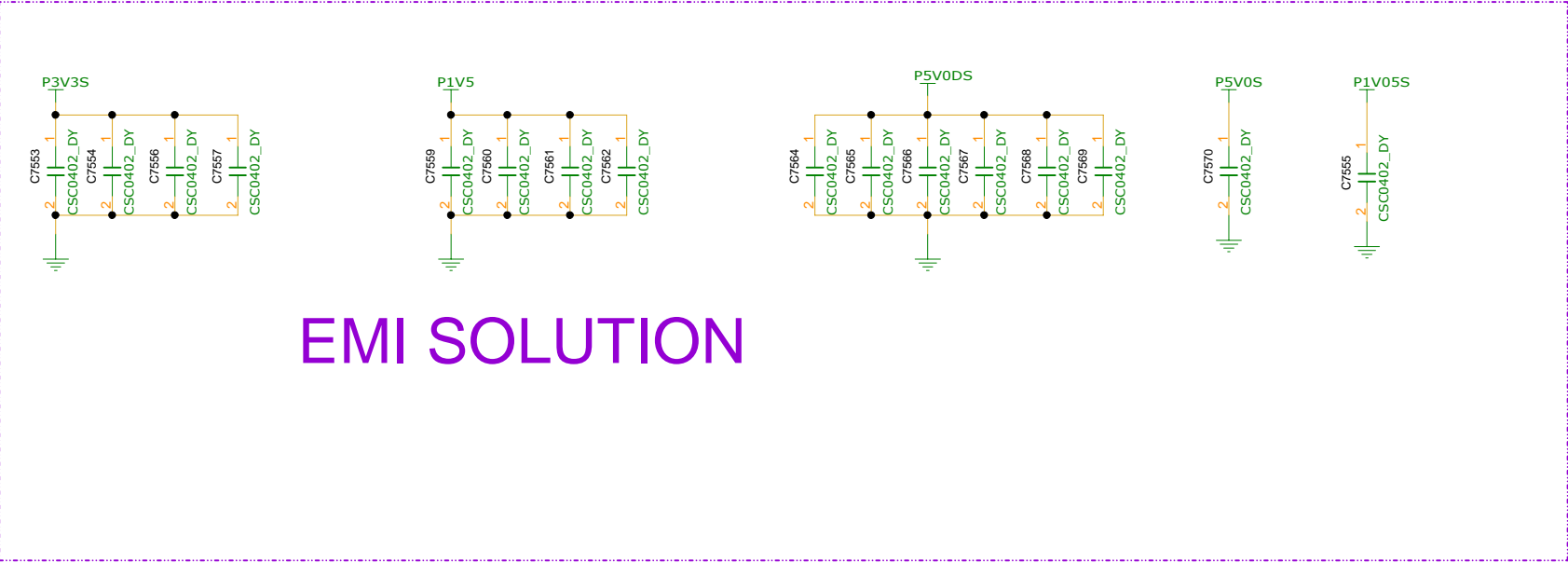
- FIX1
FIX_MASK
- FIX2
FIX_MASK
- FIX3
FIX_MASK
- FIX4
FIX_MASK
- FIX5
FIX_MASK
- FIX6
FIX_MASK
- FIX7
FIX_MASK
- FIX8
FIX_MASK

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION SCREW			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 66 of 77			

CHANGE by XXX DATE 21-OCT-2002



RF SOLUTION



EMI SOLUTION

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
EMI & RF SOLUTION			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 67 of 77			

[illegible][illegible]

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

Capacitor Value (nF) Bits [5:4]

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

Note: 0402 1% resistors are required.

THERM SENSOR

U5001 PART 2 OF 3

GENERAL PURPOSE I/O

MLPS

DOC/AUX

DEBUG

TESTEN

THERMAL

AMD_MARS_M2_FCBGA_962P

INVENTEC

MODEL PROJECT FUNCTION

AMD-THAMES-1

CODE

1310

DATE

11-01-2022

CHANGE BY

WVF

SHEET

1

REV

001

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

Capacitor Value (nF) Bits [5:4]

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

Note: 0402 1% resistors are required.

THERM SENSOR

U5001 PART 2 OF 3

GENERAL PURPOSE I/O

MLPS

DOC/AUX

DEBUG

TESTEN

THERMAL

AMD_MARS_M2_FCBGA_962P

INVENTEC

MODEL PROJECT FUNCTION

AMD-THAMES-1

CODE

1310

DATE

11-01-2022

CHANGE BY

WVF

SHEET

1

REV

001

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

Capacitor Value (nF) Bits [5:4]

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

Note: 0402 1% resistors are required.

THERM SENSOR

U5001 PART 2 OF 3

GENERAL PURPOSE I/O

MLPS

DOC/AUX

DEBUG

TESTEN

THERMAL

AMD_MARS_M2_FCBGA_962P

INVENTEC

MODEL PROJECT FUNCTION

AMD-THAMES-1

CODE

1310

DATE

11-01-2022

CHANGE BY

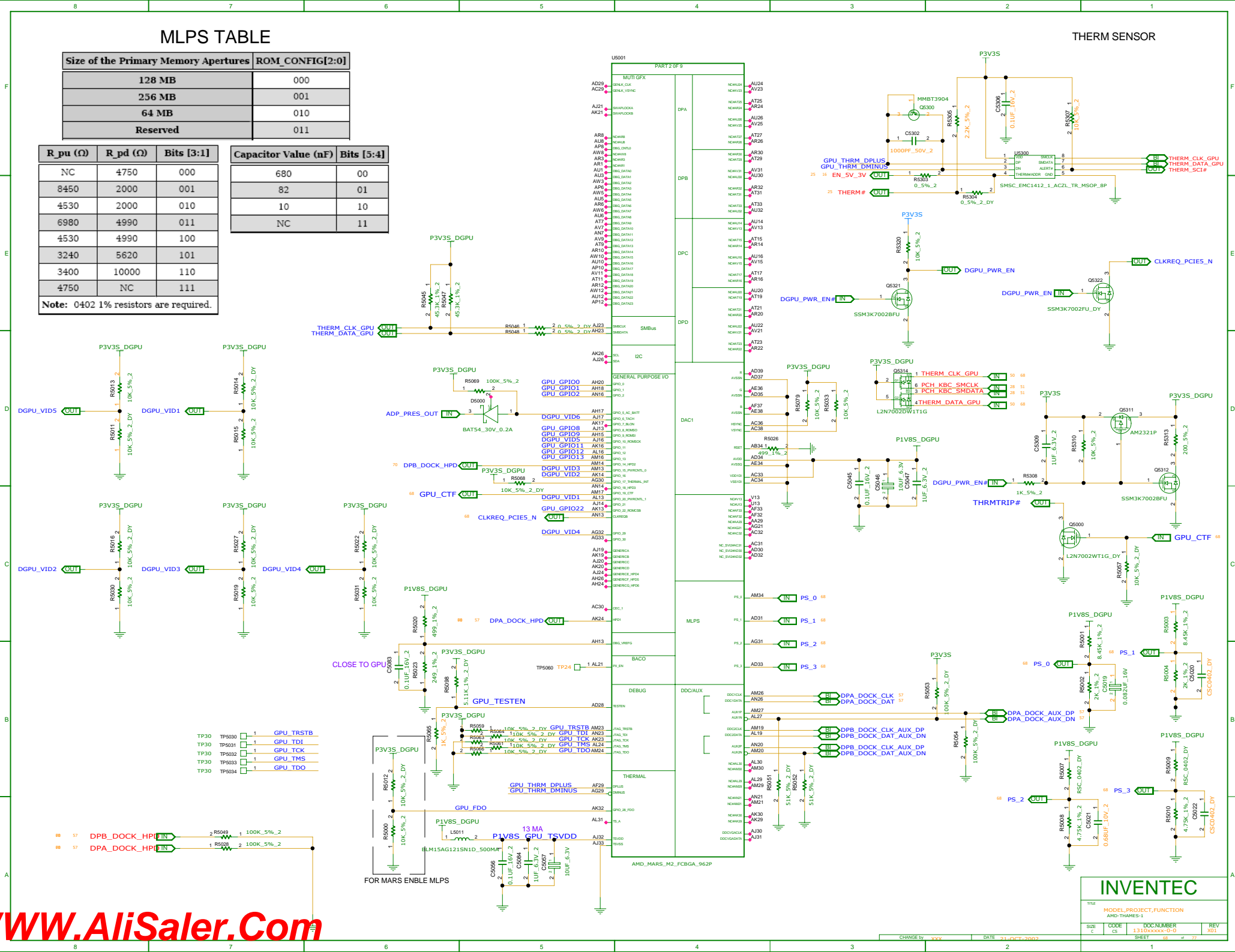
WVF

SHEET

1

REV

001



MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF) Bits [5:4]

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

THERM SENSOR

INVENTEC

MODEL: PROJECT: FUNCTION: AMD-THAMES-1

DATE: 131011-01-10

REV: 1.0

SIZE: C

CODE: 15

SHEET: 16

CHANG BY: WXX

DATE: 13-01-2012

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF) Bits [5:4]

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

THERM SENSOR

INVENTEC

MODEL: PROJECT: FUNCTION: AMD-THAMES-1

DATE: 131011-01-10

REV: 1.0

SIZE: C

CODE: 15

SHEET: 16

CHANG BY: WXX

DATE: 13-01-2012

LPT-LP GPIO 34	MARS MLPS Bit: PS_3 [3:1]			R_pu (Ω)	R_pd (Ω)	Vendor & PN	Die Ver.	
0	0	0	0	NC	4750	Samsung - K4G20325FD-FC04	D	GDDR5 - 64Mx32/128Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
	0	0	1	8450	2000	Hynix - H5GQ2H24AFR-T2C	A (Gemma)	GDDR5 - 64Mx32/128Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
1	1	1	0	3400	10000	*Samsung - K4G41325FC-HC04	C	*GDDR5 - 128Mx32/256Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
	1	1	1	4759	NC	*Hynix - H5G4C4H24MFR-T0C	Huma	*GDDR5 - 128Mx32/256Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
VBIOS selection : 0 : VBIOS 1, 64Mx32 for 1GB sku 1 : VBIOS 2, 128Mx32 for 2GB sku	Vram configuration 00: 64Mx32 (2Gb) 11: 128Mx32 (4Gb)		Vendor ID 0: Samsung 1: Hynix	Resistor Divider Lookup Table		Vram information * 2GB sku, TBD		

MLPS Implementation

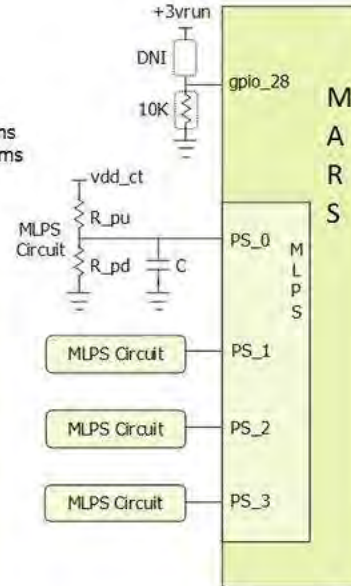
- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R _{pu} (Ohm)	R _{pd} (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111



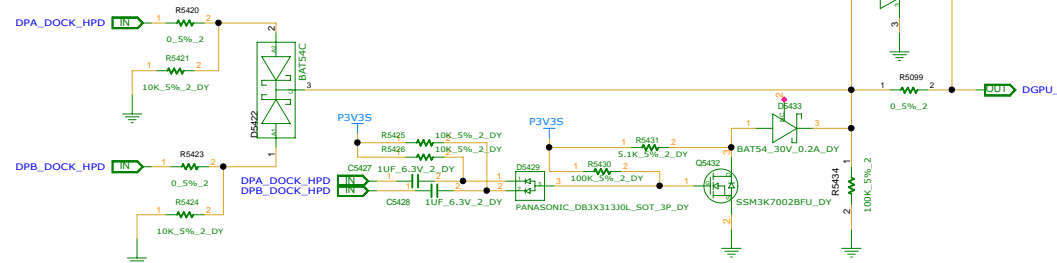
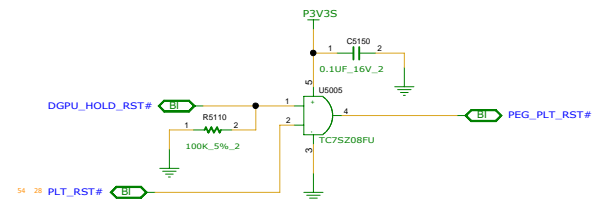
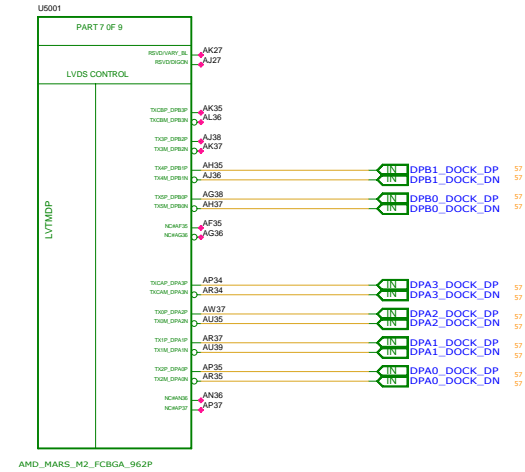
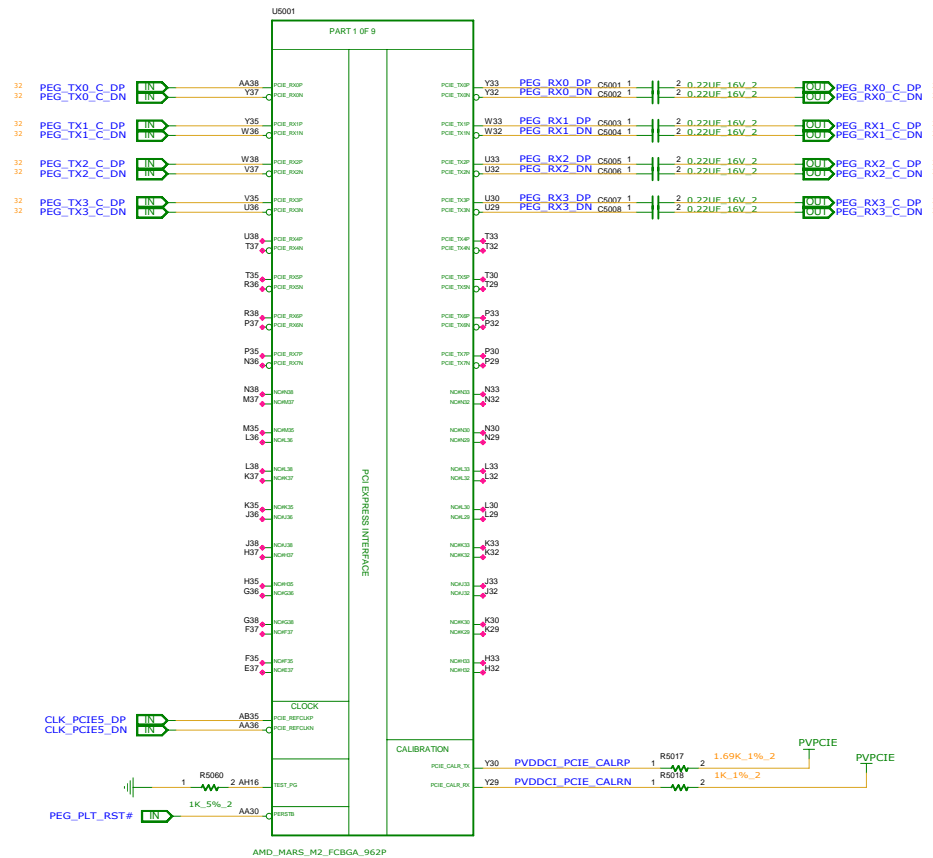
MLPS Bit	Strap Name	Description
PS_0[1]	ROM_CONFIG[0]	See Primary Memory Aperture Sizes.
PS_0[2]	ROM_CONFIG[1]	
PS_0[3]	ROM_CONFIG[2]	
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap that indicates the number of audio-capable display outputs.
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 1 = Tx deemphasis enabled.
PS_2[1]	N/A	Reserved.
PS_2[2]	N/A	Reserved.
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device.
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled.
PS_2[5]	N/A	Reserved
PS_2[1]	N/A	Reserved.
PS_2[2]	N/A	Reserved.
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device.
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). 0 = VGA controller capacity enabled.
PS_2[5]	N/A	Reserved
PS_3[1]	BOARD_CONFIG[0]	See Board configuration related strapping, such as for memory ID.
PS_3[2]	BOARD_CONFIG[1]	
PS_3[3]	BOARD_CONFIG[2]	
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	

Note : AUD[1] (on HYSNC) and AUD[0] (on VSYNC) still need to be properly pin strapped even in a MLPS-based design.

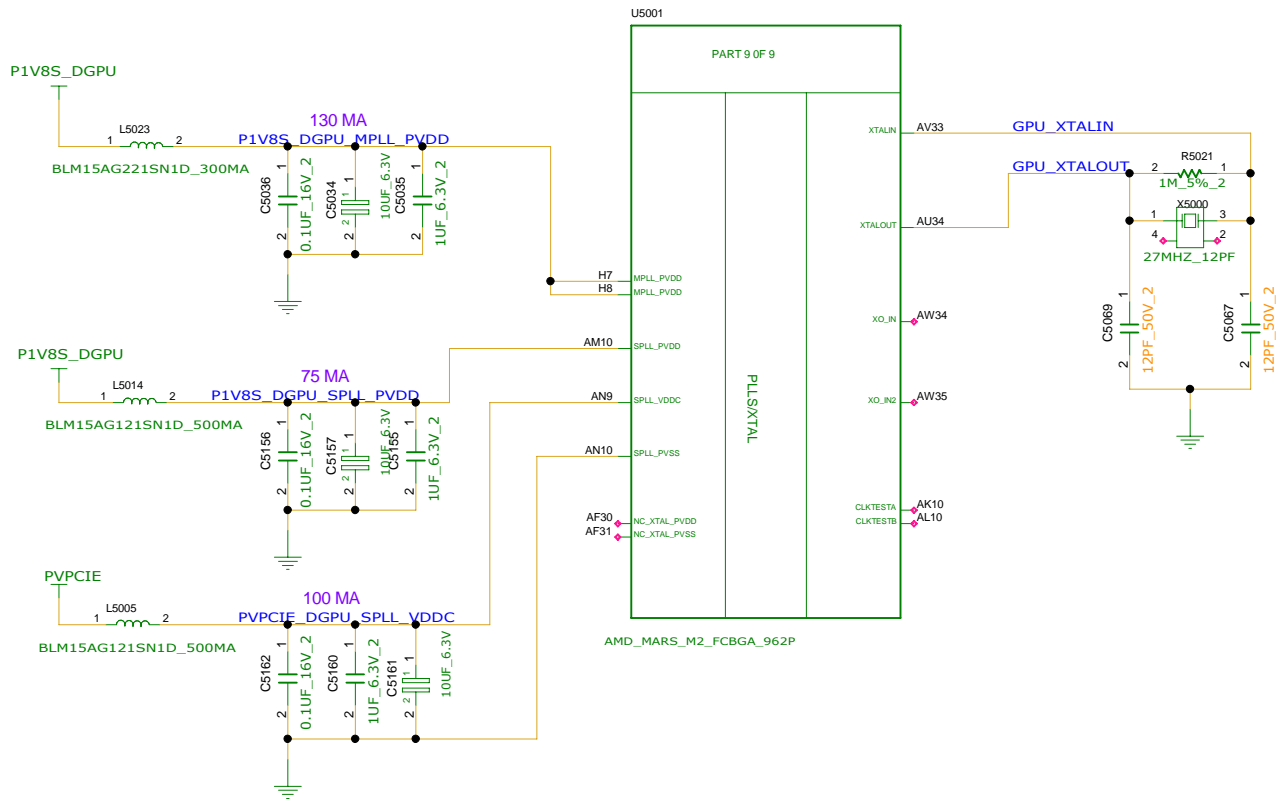
Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_0[5]	aud_port_cp[0]			

INVENTEC

TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE C	CODE CS	DOC NUMBER 1310XXXX-0-0	REV 201
SHEET 08		of 07	



INVENTEC				
MODEL,PROJECT,FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
C	CS	1310VXXXX-0-0	2021	
SHEET		36	of 37	

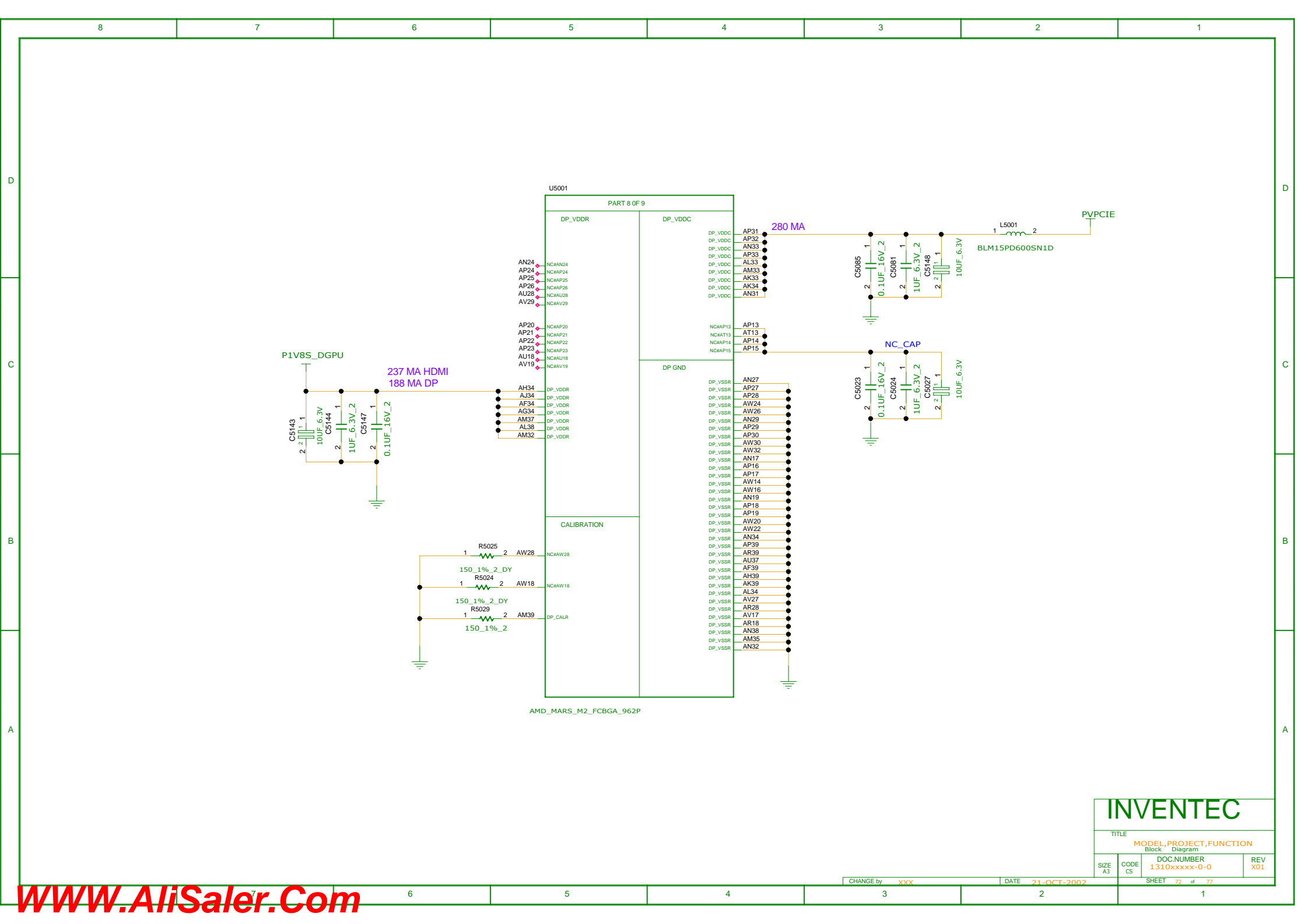


INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 71 of 77

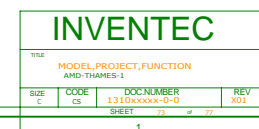


INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

CHANGE by XXX DATE 21-OCT-2002 SHEET 72 of 77



VM_DQB0_<31..0>

VM_DQB1_<31..0>

P1V35S_DGPU

P1V35S_DGPU

AMD_MARS_M2_FCBGA_962P

U5001

PART 4 OF 9

GDDBS/DDR3

MEMORY INTERFACE B

MAB0_0MAB0_0
MAB0_1MAB0_1
MAB0_2MAB0_2
MAB0_3MAB0_3
MAB0_4MAB0_4
MAB0_5MAB0_5
MAB0_6MAB0_6
MAB0_7MAB0_7
MAB0_8MAB0_8
MAB1_1MAB1_1
MAB1_2MAB1_2
MAB1_3MAB1_3
MAB1_4MAB1_4
MAB1_5BA2
MAB1_6BA0
MAB1_7BA1

WCKB0_0DQMB_0
WCKB0B_0DQMB_1
WCKB0_1DQMB_2
WCKB0B_1DQMB_3
WCKB1_0DQMB_4
WCKB1B_0DQMB_5
WCKB1_1DQMB_6
WCKB1B_1DQMB_7

EDCB0_0QSB_0
EDCB0_1QSB_1
EDCB0_2QSB_2
EDCB0_3QSB_3
EDCB1_0QSB_4
EDCB1_1QSB_5
EDCB1_2QSB_6
EDCB1_3QSB_7

DDBB0_0QSB_0B
DDBB0_1QSB_1B
DDBB0_2QSB_2B
DDBB0_3QSB_3B
DDBB1_0QSB_4B
DDBB1_1QSB_5B
DDBB1_2QSB_6B
DDBB1_3QSB_7B

ADB0_0DTB0
ADB1_0DTB1

CLKB0
CLKB0B

CLKB1
CLKB1B

RASB0B
RASB1B

CASB0B
CASB1B

CSB0B_0
CSB0B_1

CSB1B_0
CSB1B_1

CKEB0
CKEB1

WEB0B
WEB1B

MAB0_8MAB0_13
MAB1_8MAB1_14
MAB0_9MAB0_15
MAB1_9RSVD

DRAM_RST

P8 VM MAB0 <0>
T9 VM MAB0 <1>
P9 VM MAB0 <2>
N7 VM MAB0 <3>
N8 VM MAB0 <4>
N9 VM MAB0 <5>
U8 VM MAB0 <6>
Y9 VM MAB1 <0>
W9 VM MAB1 <1>
AC8 VM MAB1 <2>
AC9 VM MAB1 <3>
AA7 VM MAB1 <4>
Y8 VM MAB1 <5>
Y8 VM MAB1 <6>
AA9 VM MAB1 <7>

H3
H1
T3
T5
AE4
AF5
AK6
AK5

F6
K3
P3
V5
AB5
AH1
AJ9
AM5

G7
K1
P1
W4
AC4
AH3
AJ8
AM3

T7
W7

L9
L8

AD8
AD7

T10
Y10

W10
AA10

P10
L10

AD10
AC10

U10
AA11

N10
AB11

T8
W8

U12
V12

VM MAB0 <7..0>
VM MAB1 <7..0>

VM WCKB0_0 DP
VM WCKB0_0 DN
VM WCKB0_1 DP
VM WCKB0_1 DN
VM WCKB1_0 DP
VM WCKB1_0 DN
VM WCKB1_1 DP
VM WCKB1_1 DN

VM EDCB0_0
VM EDCB0_1
VM EDCB0_2
VM EDCB0_3
VM EDCB1_0
VM EDCB1_1
VM EDCB1_2
VM EDCB1_3

VM DDBIB0_0
VM DDBIB0_1
VM DDBIB0_2
VM DDBIB0_3
VM DDBIB1_0
VM DDBIB1_1
VM DDBIB1_2
VM DDBIB1_3

VM ADBIB0_77
VM ADBIB1_77

VM CLKB0_DP
VM CLKB0_DN
VM CLKB1_DP
VM CLKB1_DN

VM RASB0#
VM RASB1#

VM CASB0#
VM CASB1#

VM CSB0#_0
VM CSB1#_0

VM CKEB0_77
VM CKEB1_77

VM WEB0_77
VM WEB1_77

VM MAB0 <8>
VM MAB1 <8>

DRAM_RST# 76 77

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
AMD THAMES-3			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01

